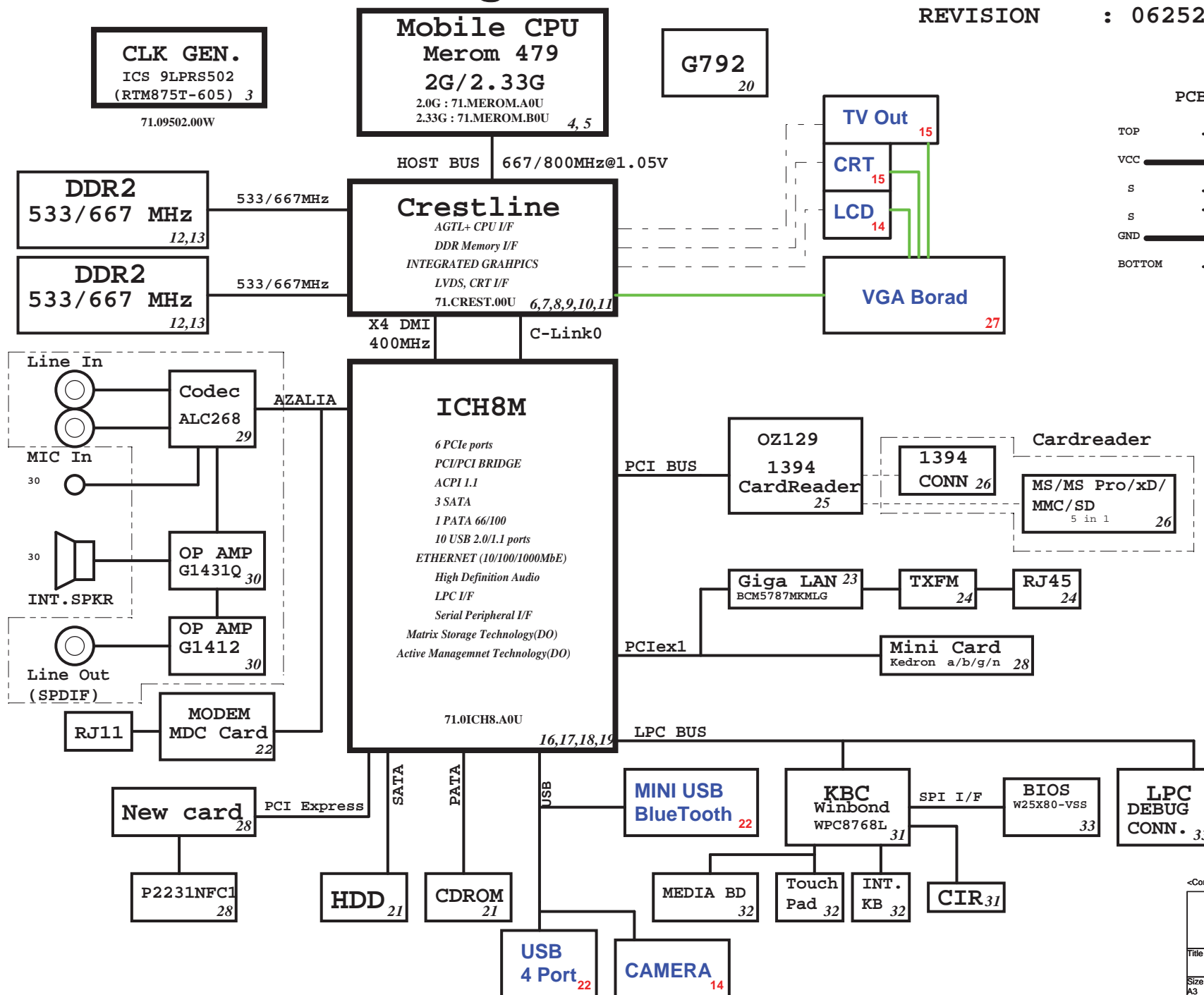


Tahoe Block Diagram

Project code: 91.4T901.001
PCB P/N : 48.4T901.0SA
REVISION : 06252-SA



SYSTEM DC/DC MAX8744 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (7A)
SYSTEM DC/DC Max8717 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (9.5A) 1D8V_S3 (8.5A)
TPS51100 41	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5915 41	
1D8V_S3	1D25V_S0 (2A)
APL531230	
3D3V_S0	2D5V_S0 (300mA)
APW5912 40	
3D3V_S5	1D5V_S3 (7.5A)
CHARGER MAX8731 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	FT
4	USB3
5	BLUETOOTH
6	NC
7	MINICARD
8	WEBCAM
9	Reserved

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ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0
page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWORK in signal.

UMA

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Title	
Reference	
Size A3	Document Number
Tahoe	
Date: Friday, April 27, 2007	Sheet 2 of 44
Rev -1	

6 H_A#(35..3) <<>> H_A#(35..3)

6 H_ADSTB#0 <<>> H_REQ#(4..0)

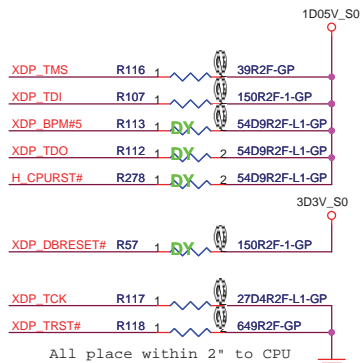
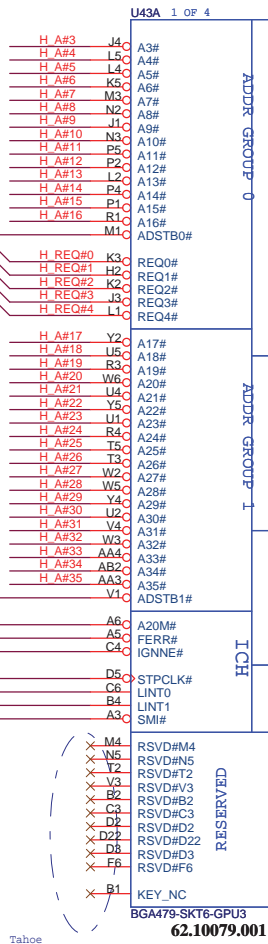
6 H_ADSTB#1 <<>> H_A20M#

16 H_A20M# <<>> H_FERR#

16 H_STPCLK# <<>> H_INTR#

16 H_INTR# <<>> H_NMI#

16 H_NMI# <<>> H_SMI#



Place testpoint on H_IERR# with a GND 0.1" away

Layout Note:
"CPU_GTLREF0"
0.5" max length.

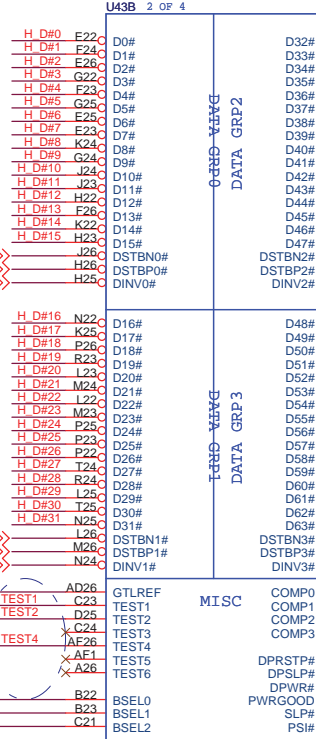
Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals

H_DINV#(3..0) <<>> H_DINV#(3..0) 6

H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6

H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6

H_D#(63..0) <<>> H_D#(63..0) 6



Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5"

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Title		CPU (1 of 2)	
Size	Document Number	Tahoe	
Date	Friday, April 27, 2007	Sheet	4 of 44

VCC_CORE_S0

VCC_CORE_S0

VCC_CORE_S0

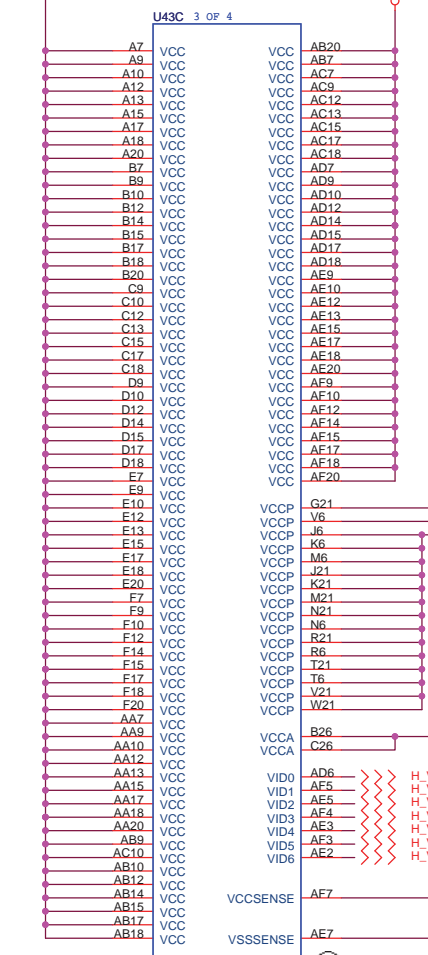
VCC_CORE_S0

1D05V_S0

1D5V_VCCA_S0

1D5V_S0

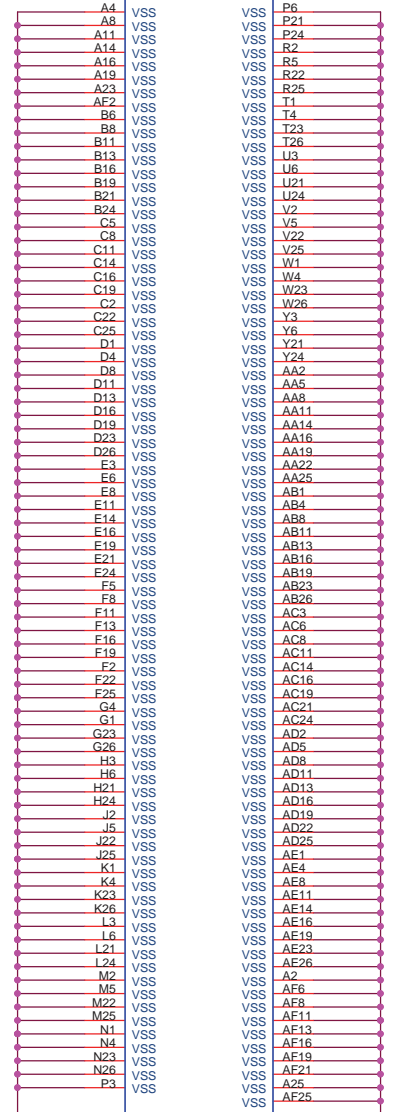
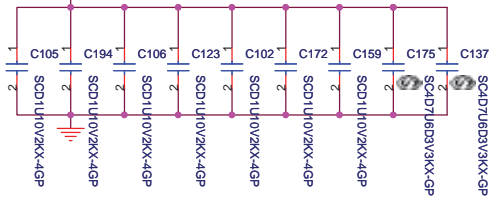
U43D 4 OF 4

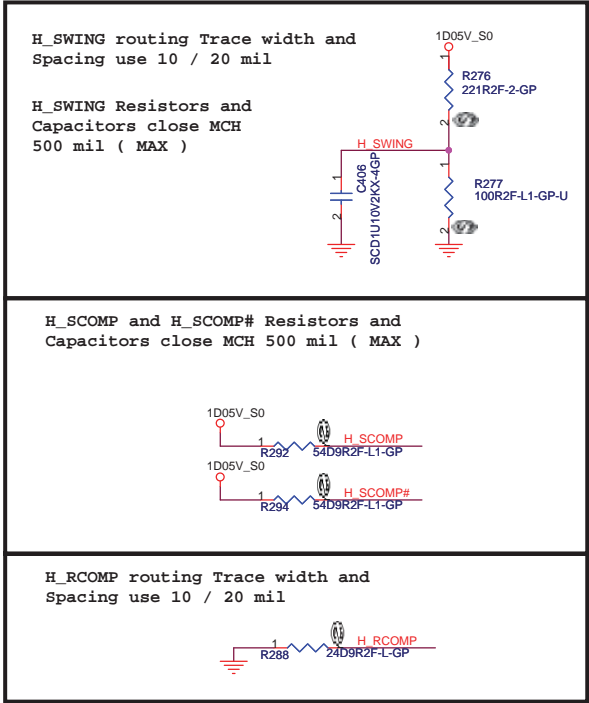


layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

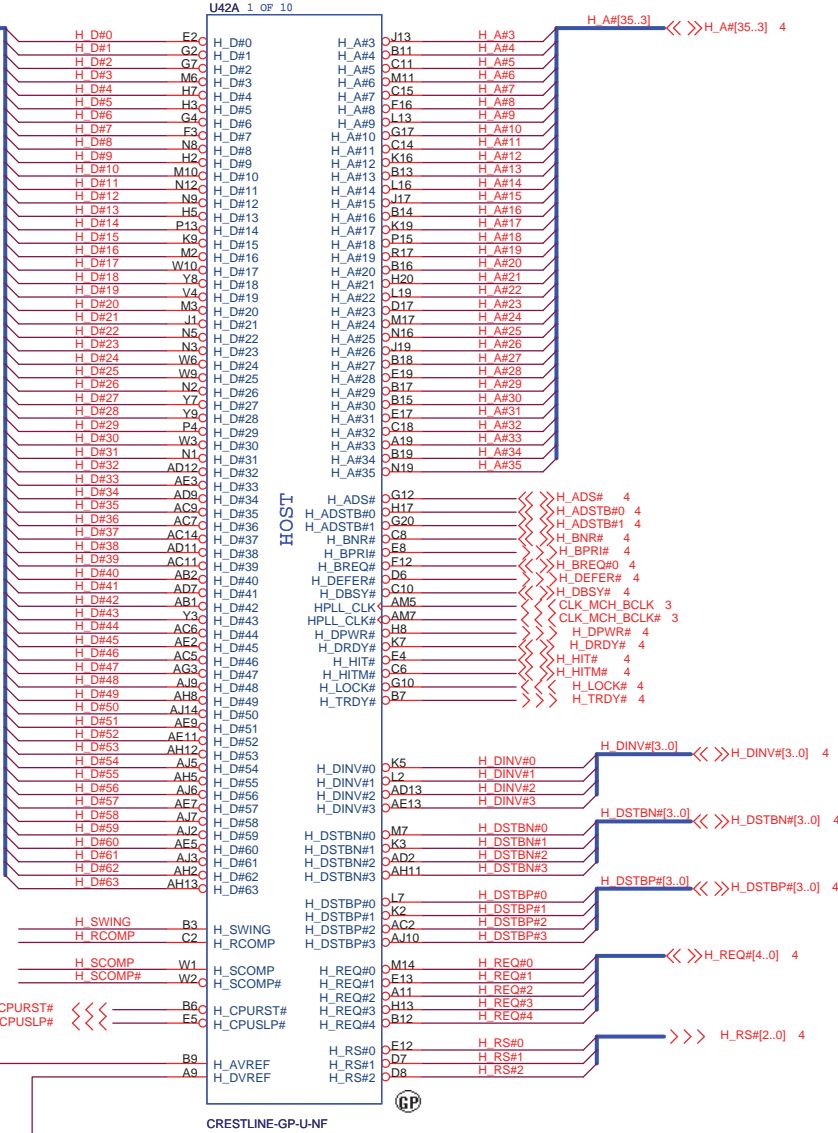
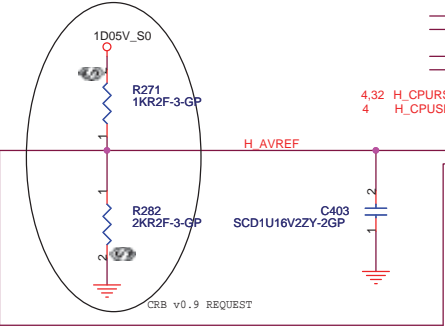
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.



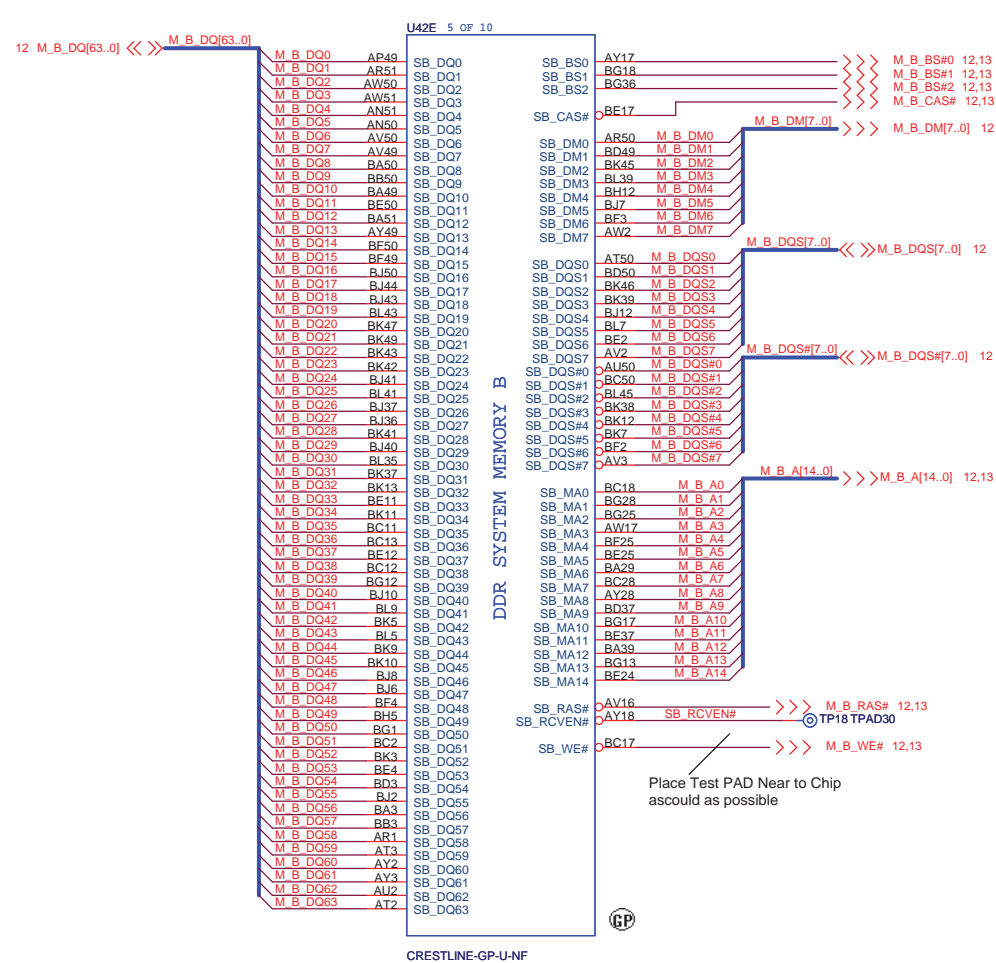


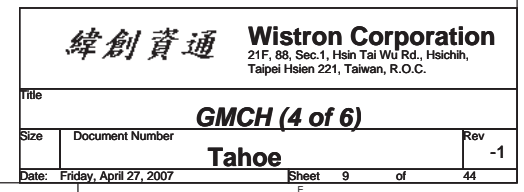
Place them near to the chip (< 0.5")

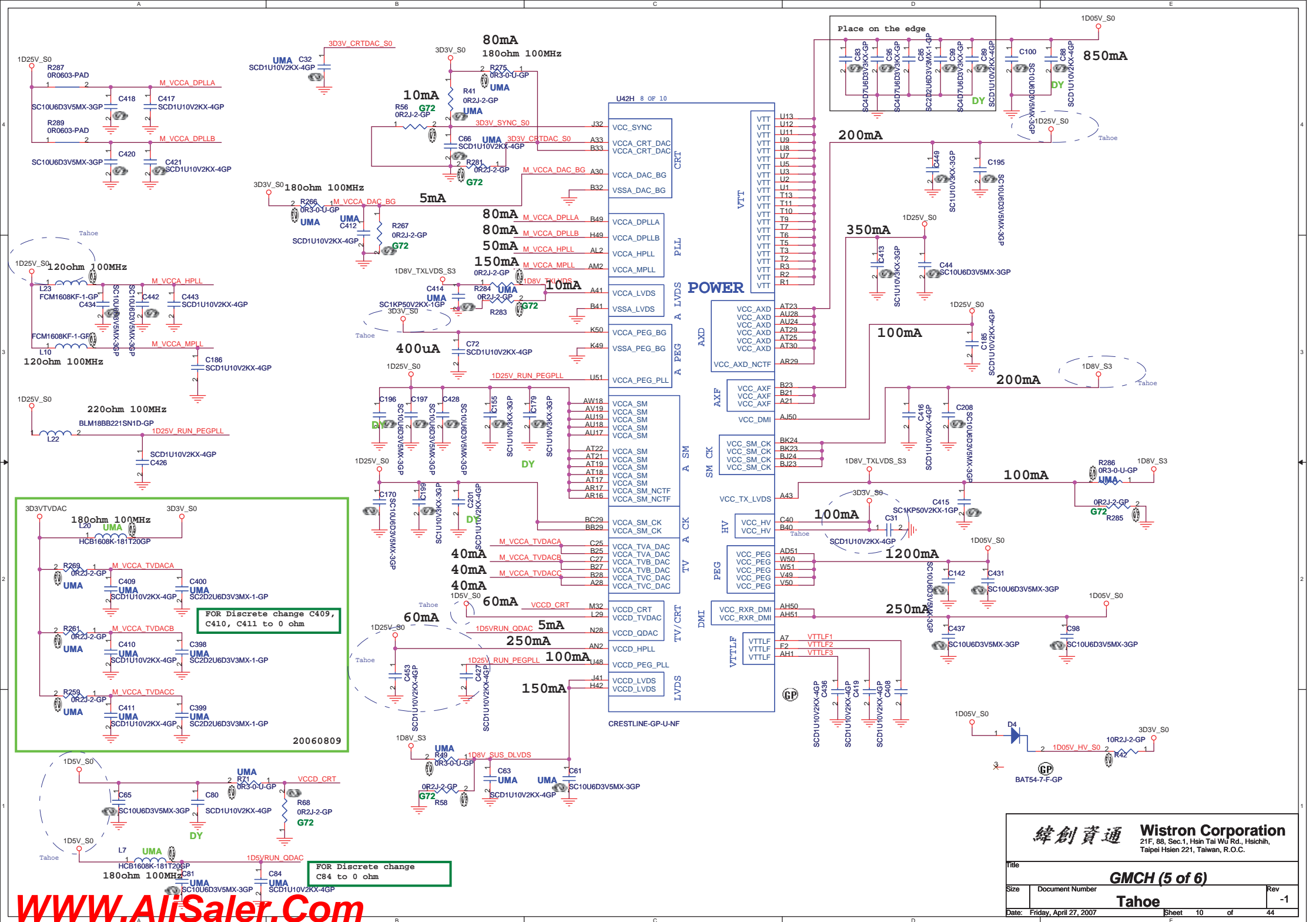
H_REF Decoupling Crestline close Crestline 100 mil





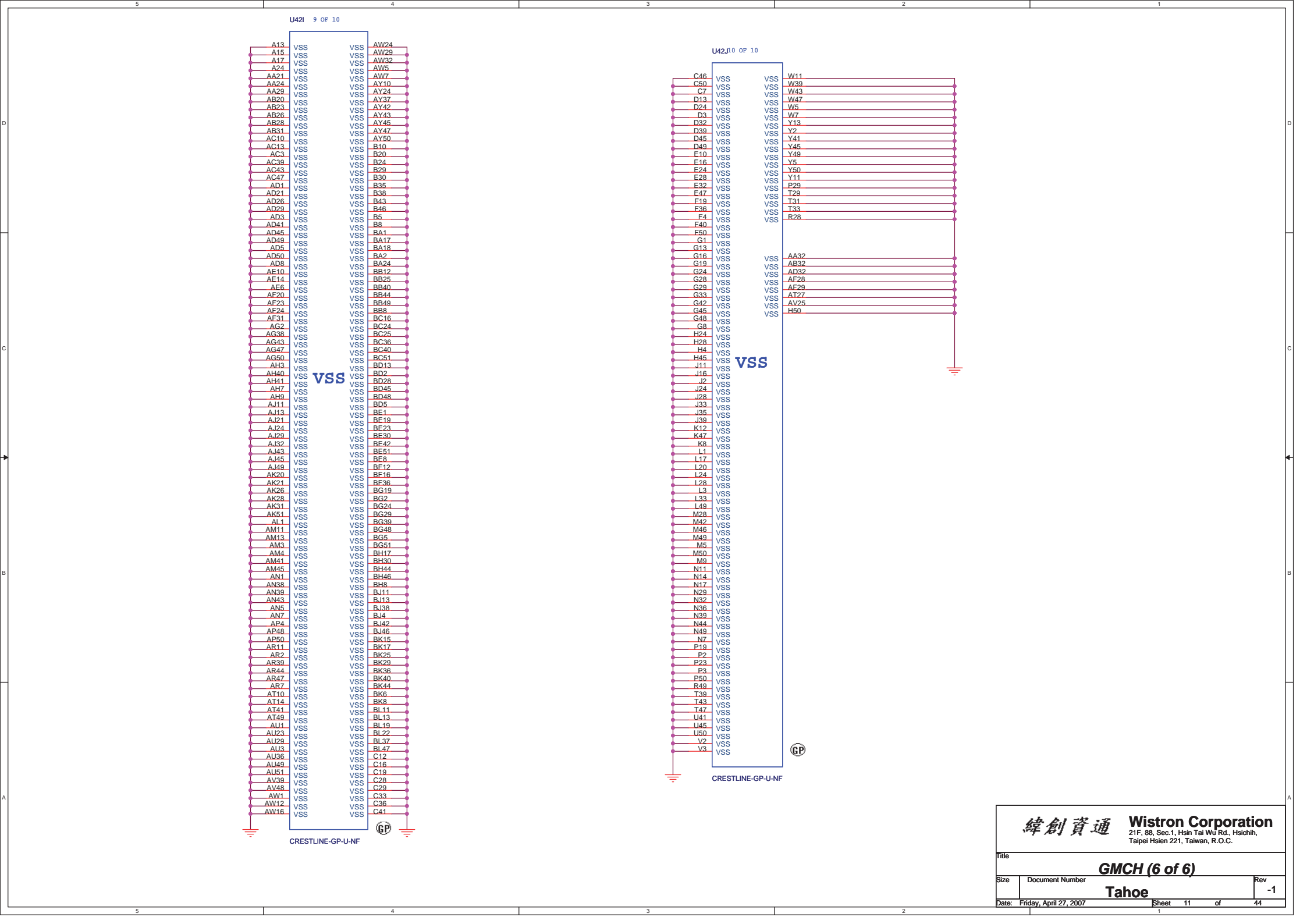




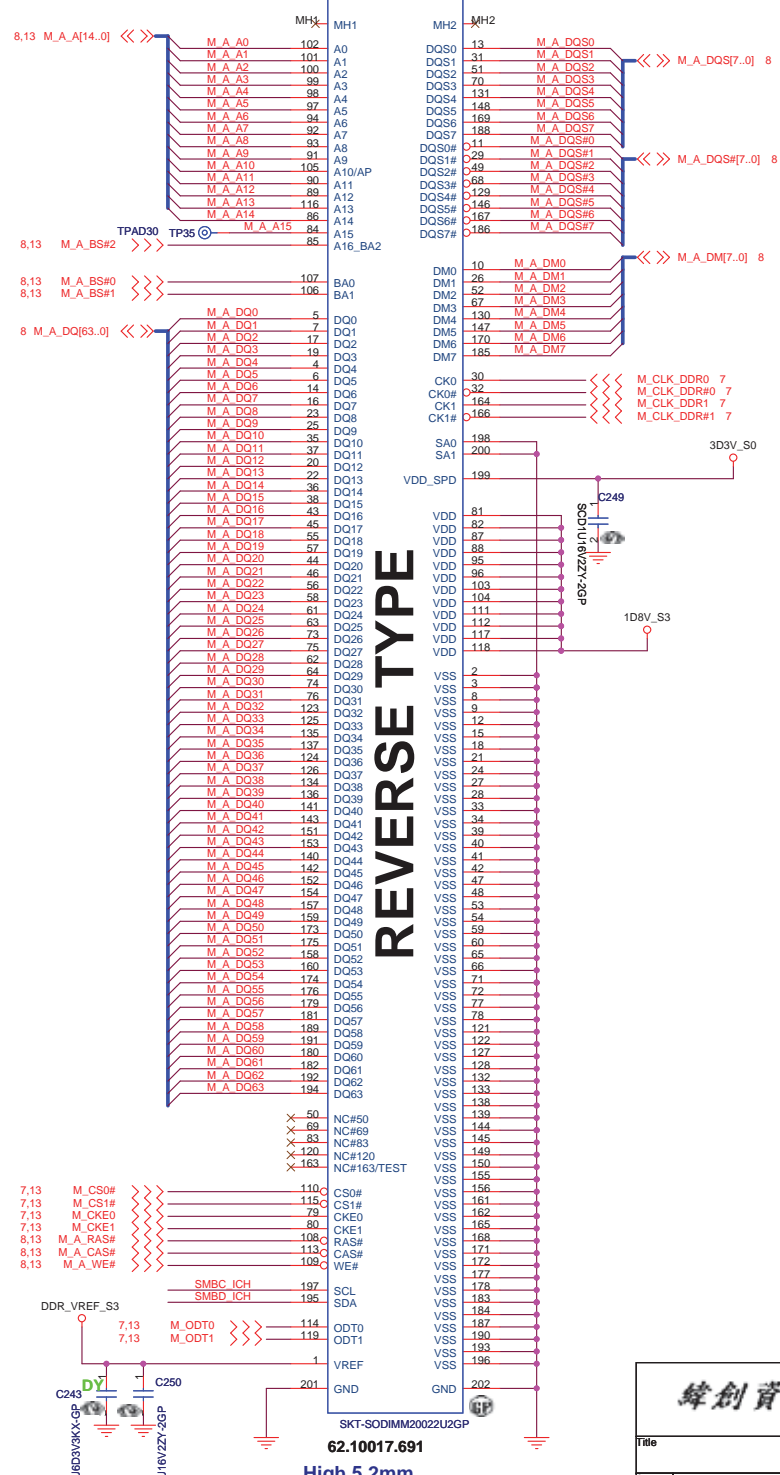


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Title			GMCH (5 of 6)	
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REVERSE TYPE



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Title

DDR2 Socket

Size

Document Number

Rev

Date

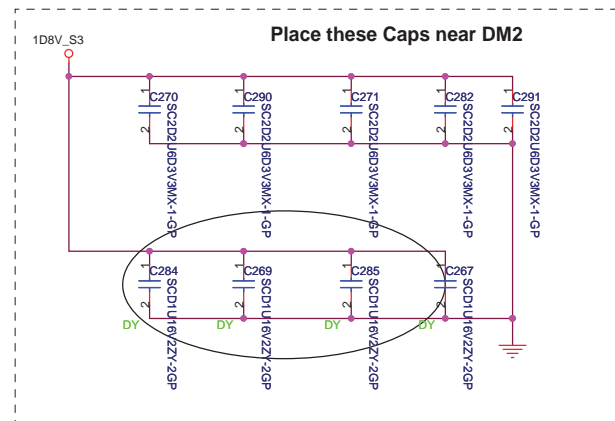
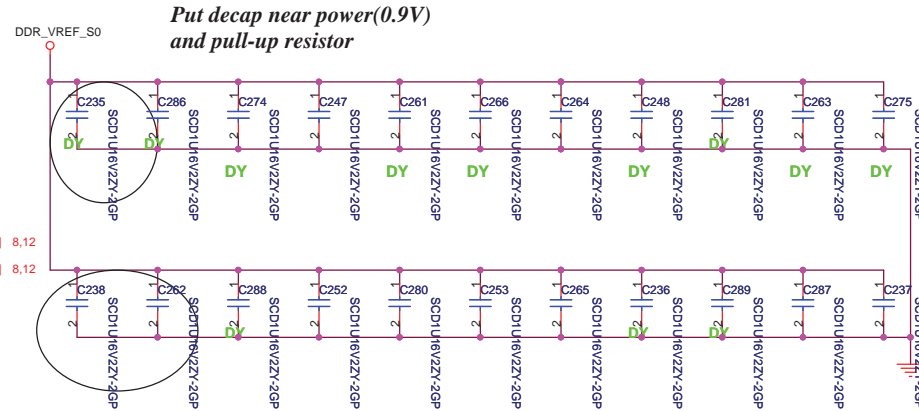
Friday, April 27, 2007

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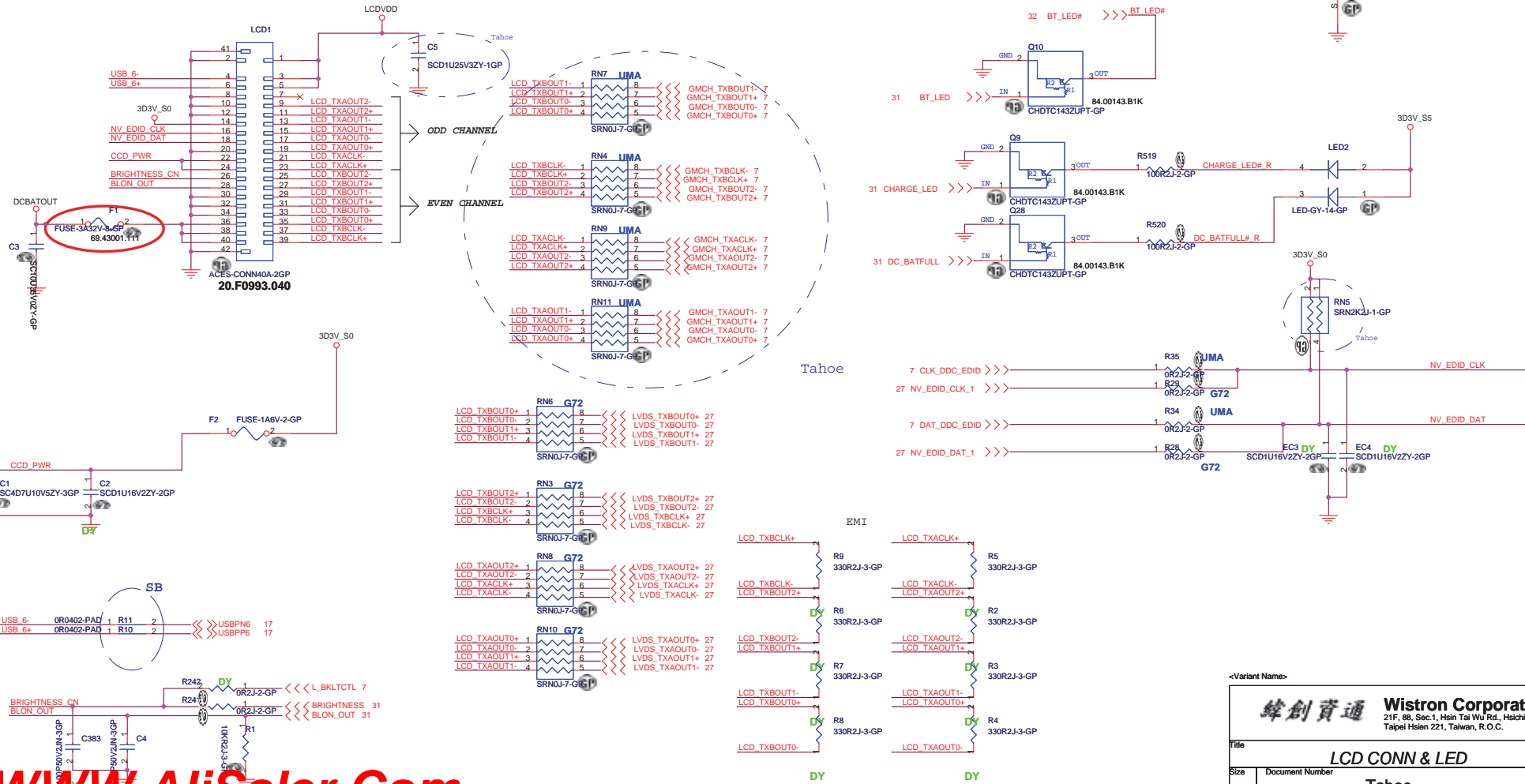
Tahoe

-1

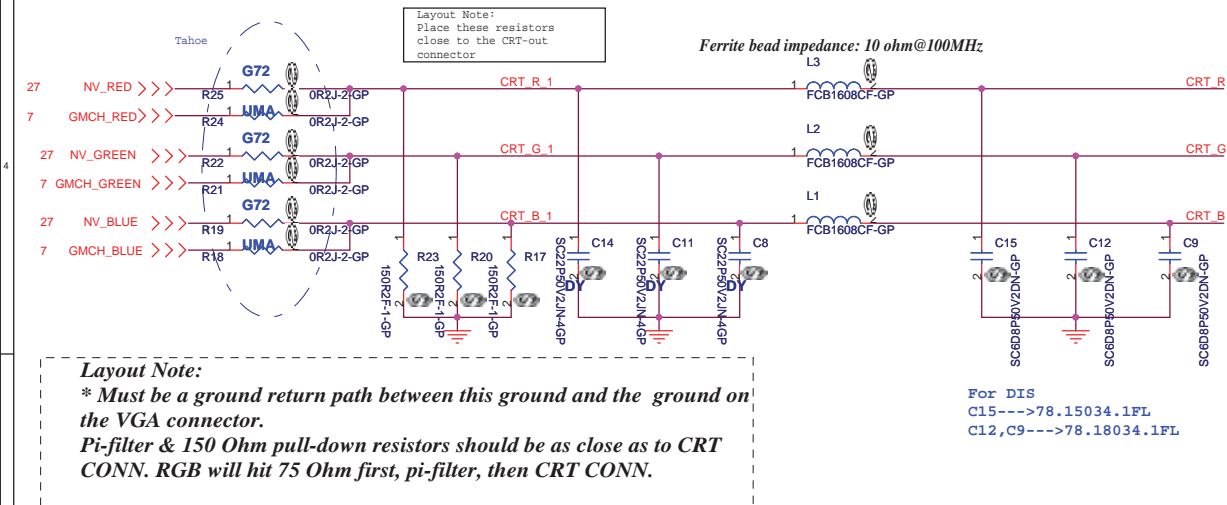
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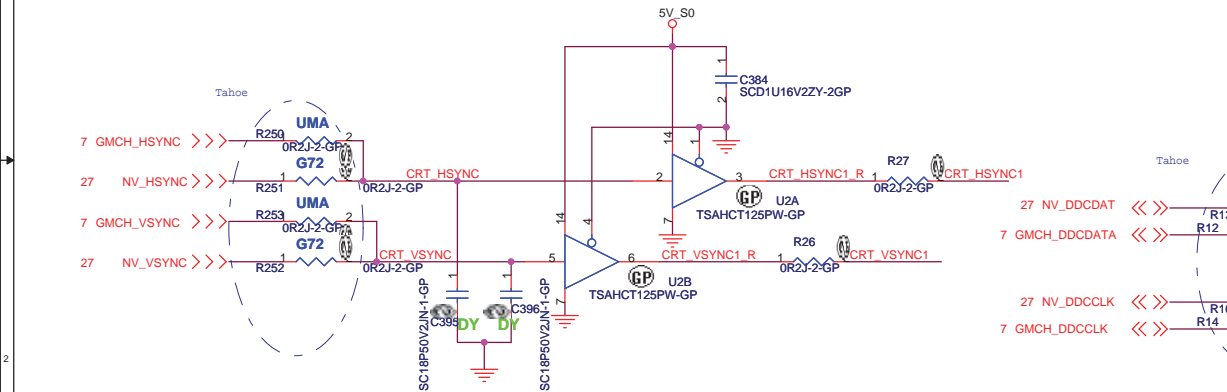
LCD/INVERTER CONN



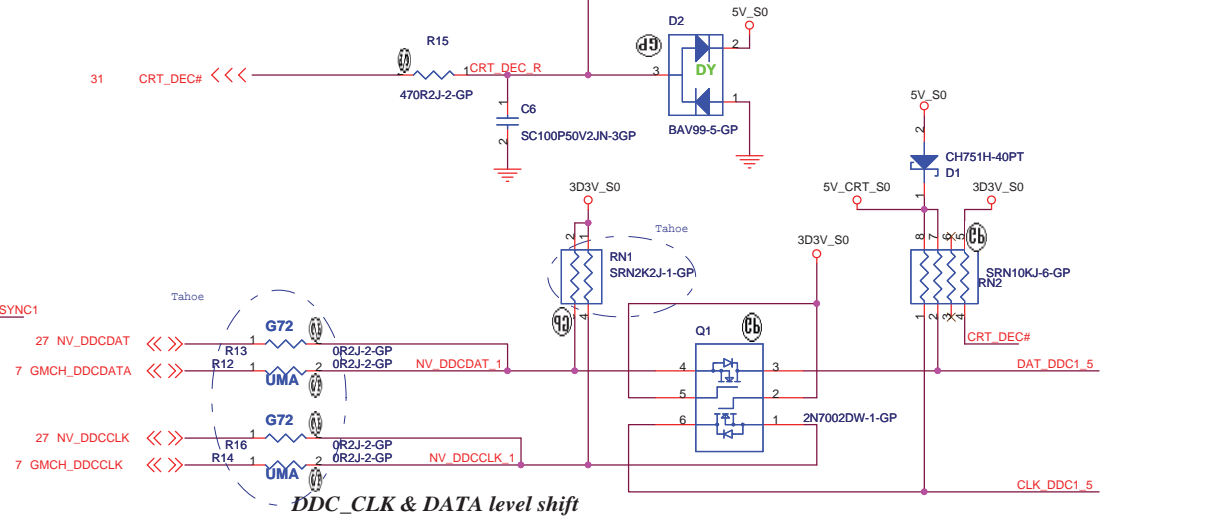
CRT I/F & CONNECTOR



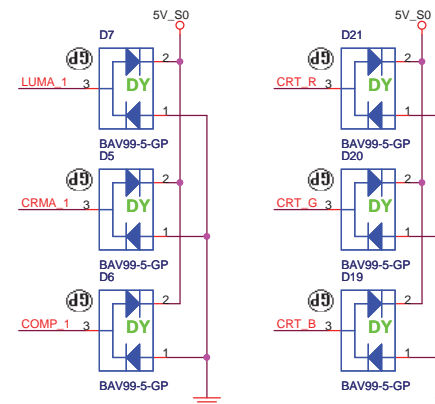
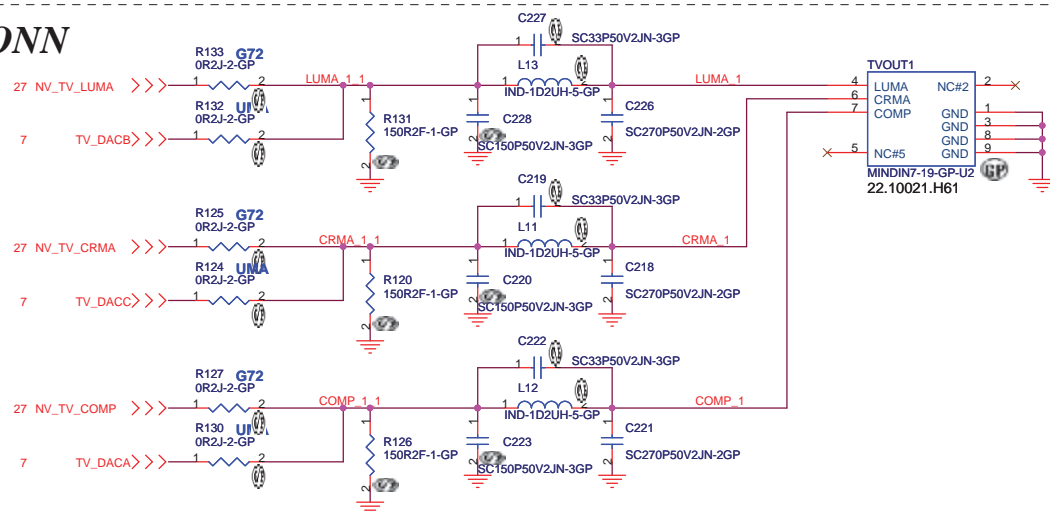
Hsync & Vsync level shift

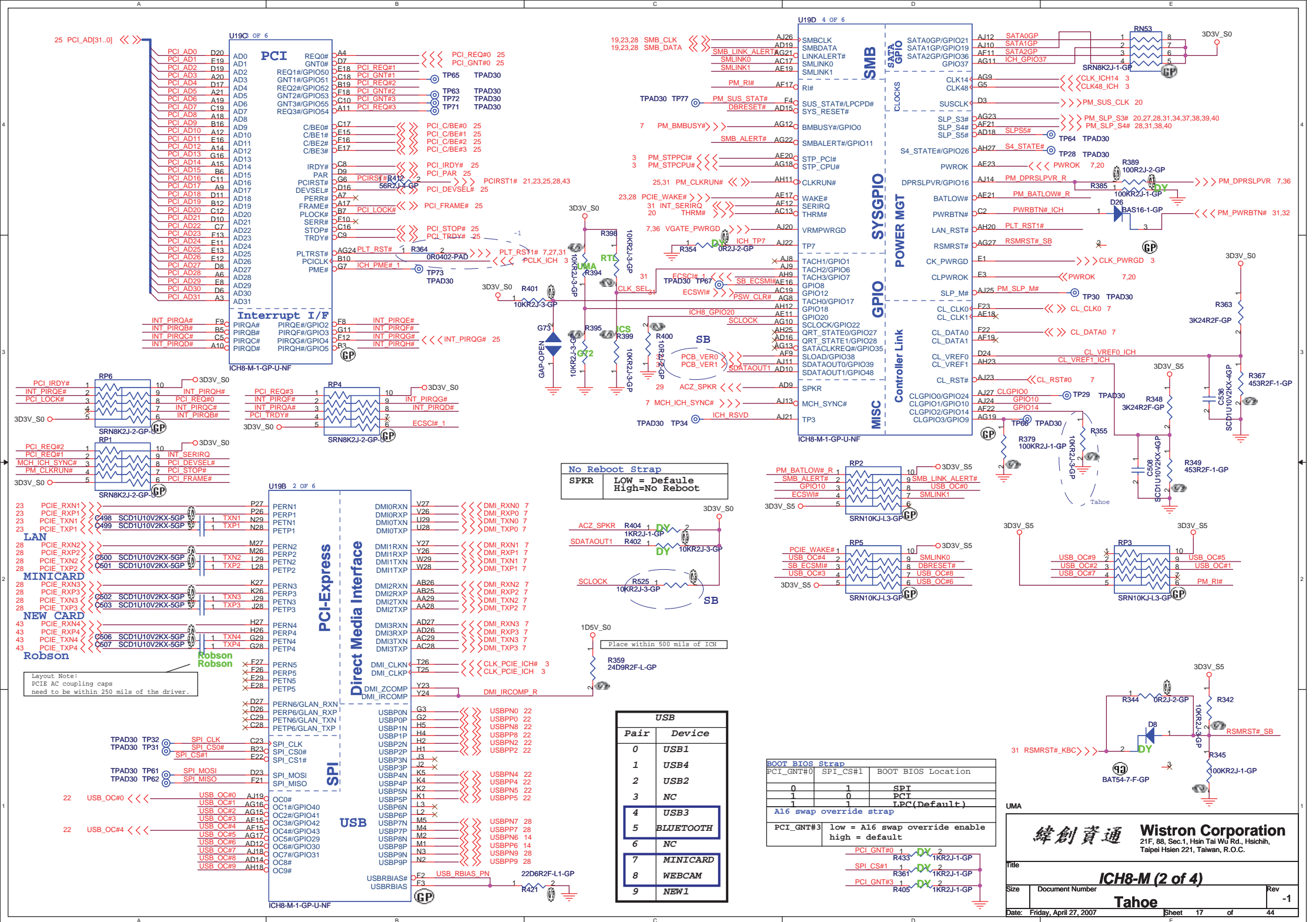


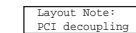
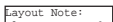
DDC_CLK & DATA level shift

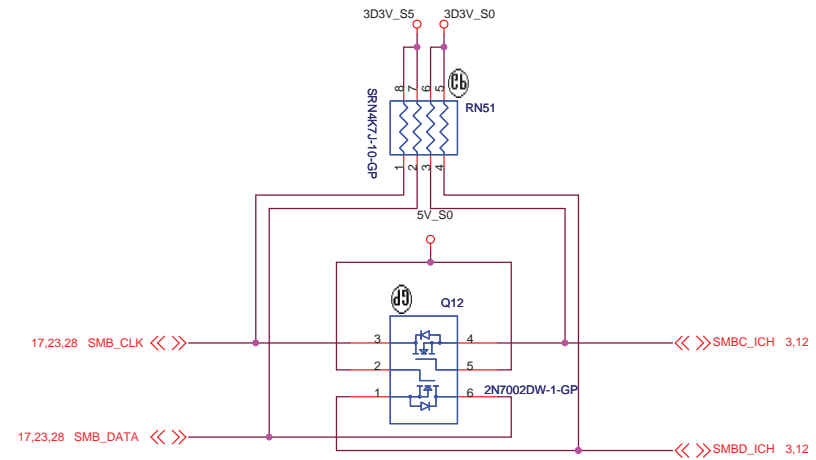
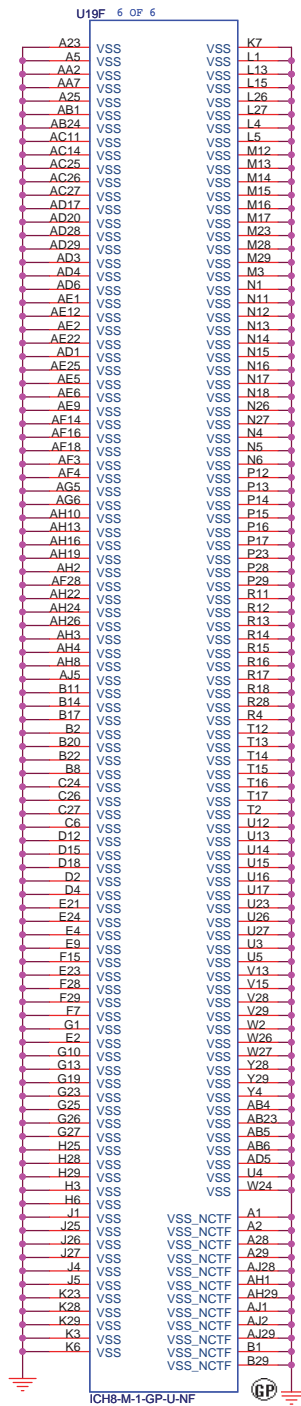


TV CONN





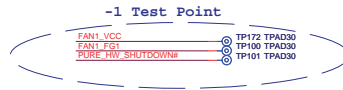




Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

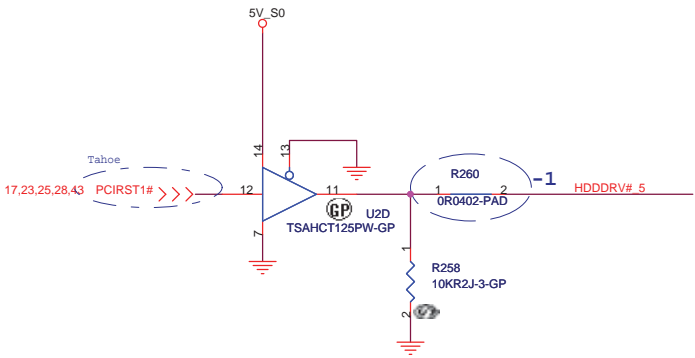
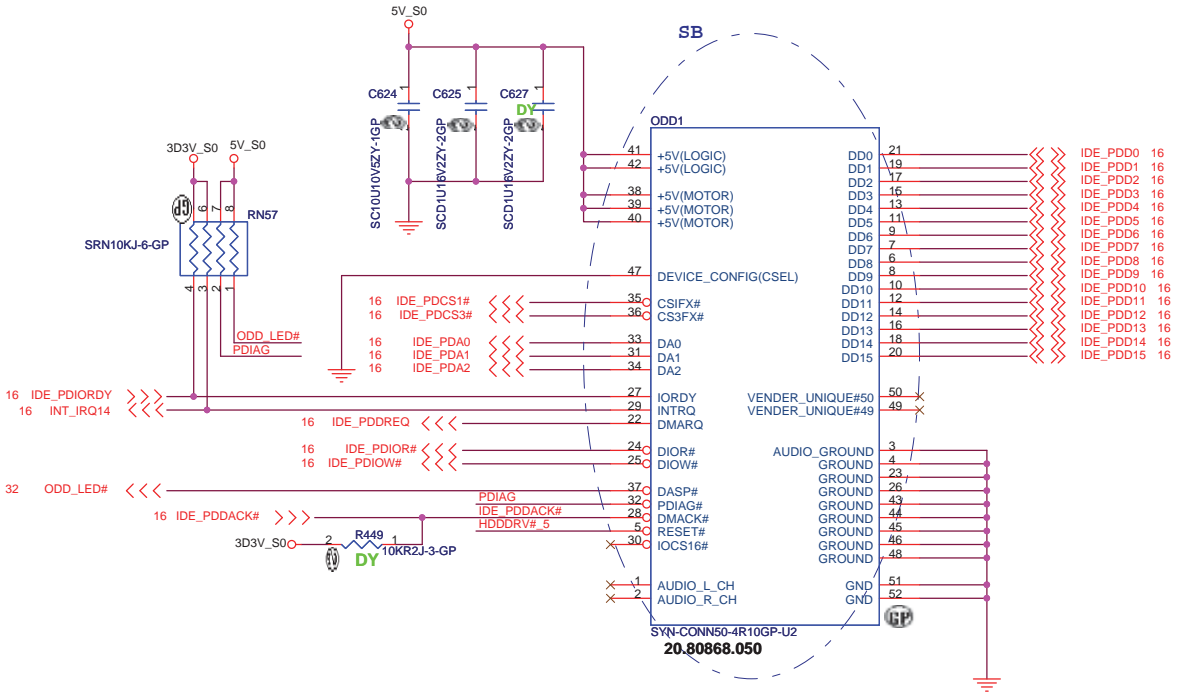
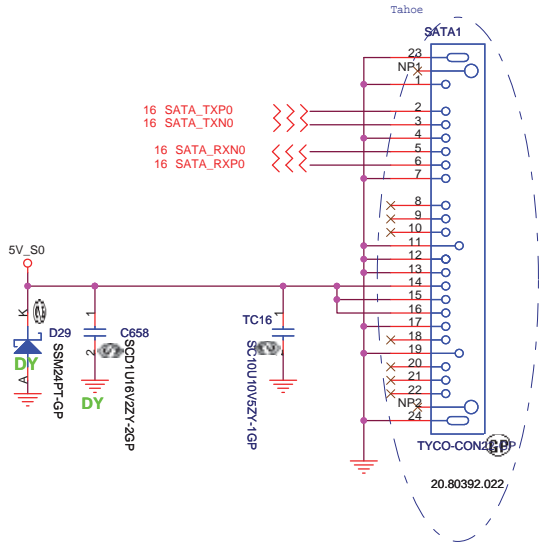
SMBUS

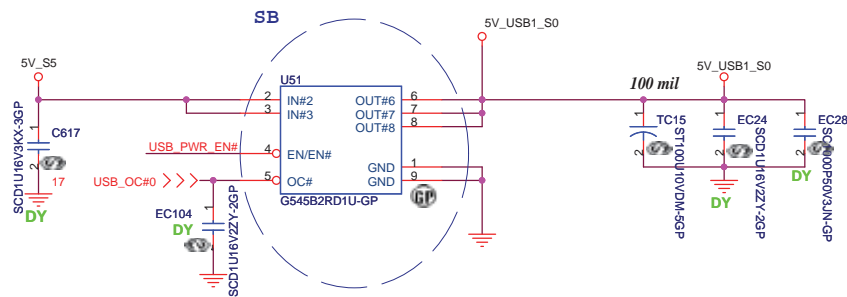
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SATA HD Connector

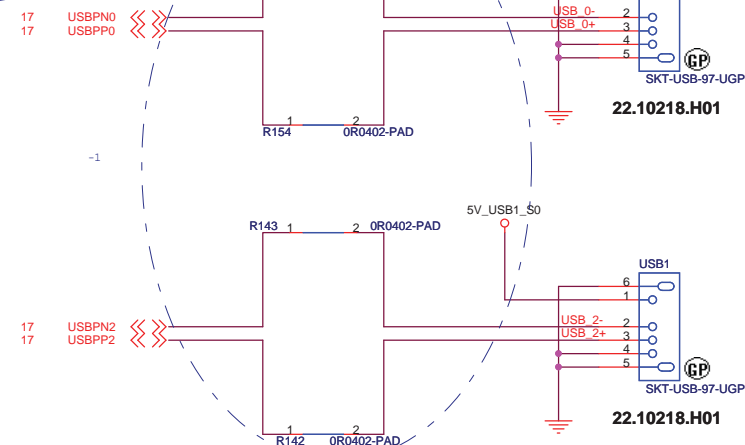
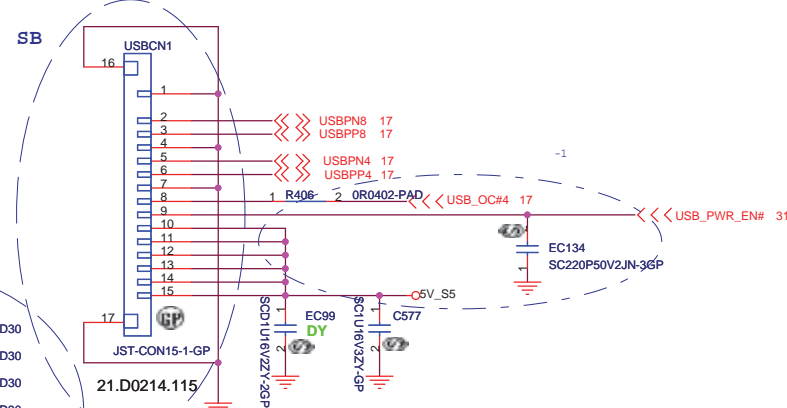
ODD Connector



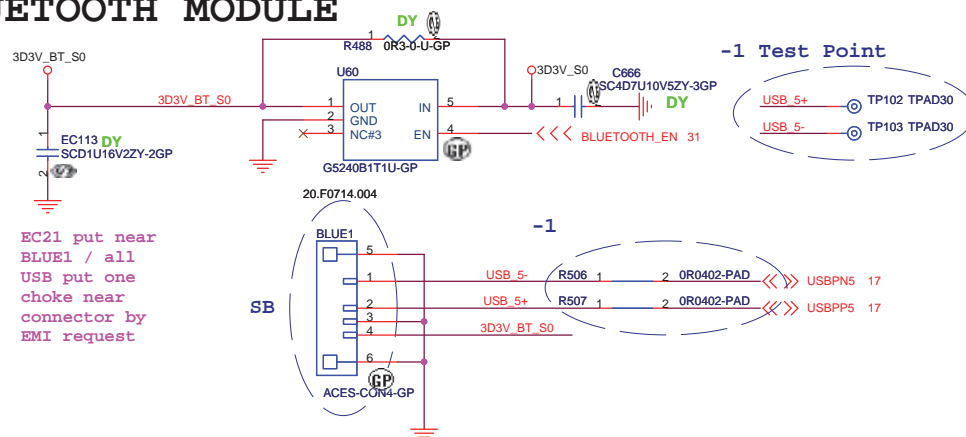


-1 Test Point

- 5V_S5 TP176 TPAD30
- 5V_S5 TP175 TPAD30
- USBP8 TP104 TPAD30
- USBP8 TP105 TPAD30
- USBP4 TP106 TPAD30
- USBP4 TP107 TPAD30
- USB_OC#4 TP108 TPAD30
- USB_PWR_EN# TP109 TPAD30

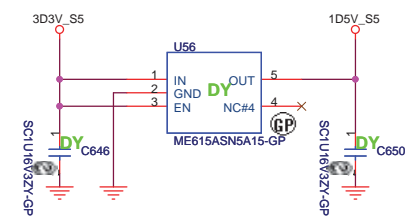
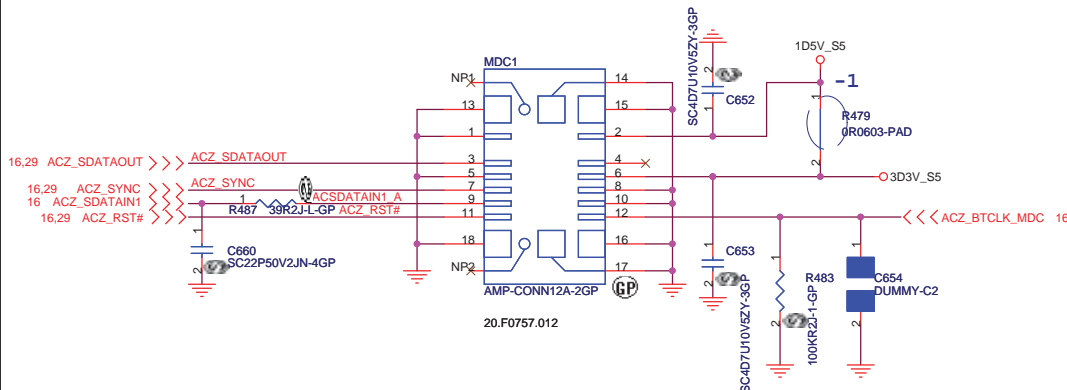


BLUETOOTH MODULE



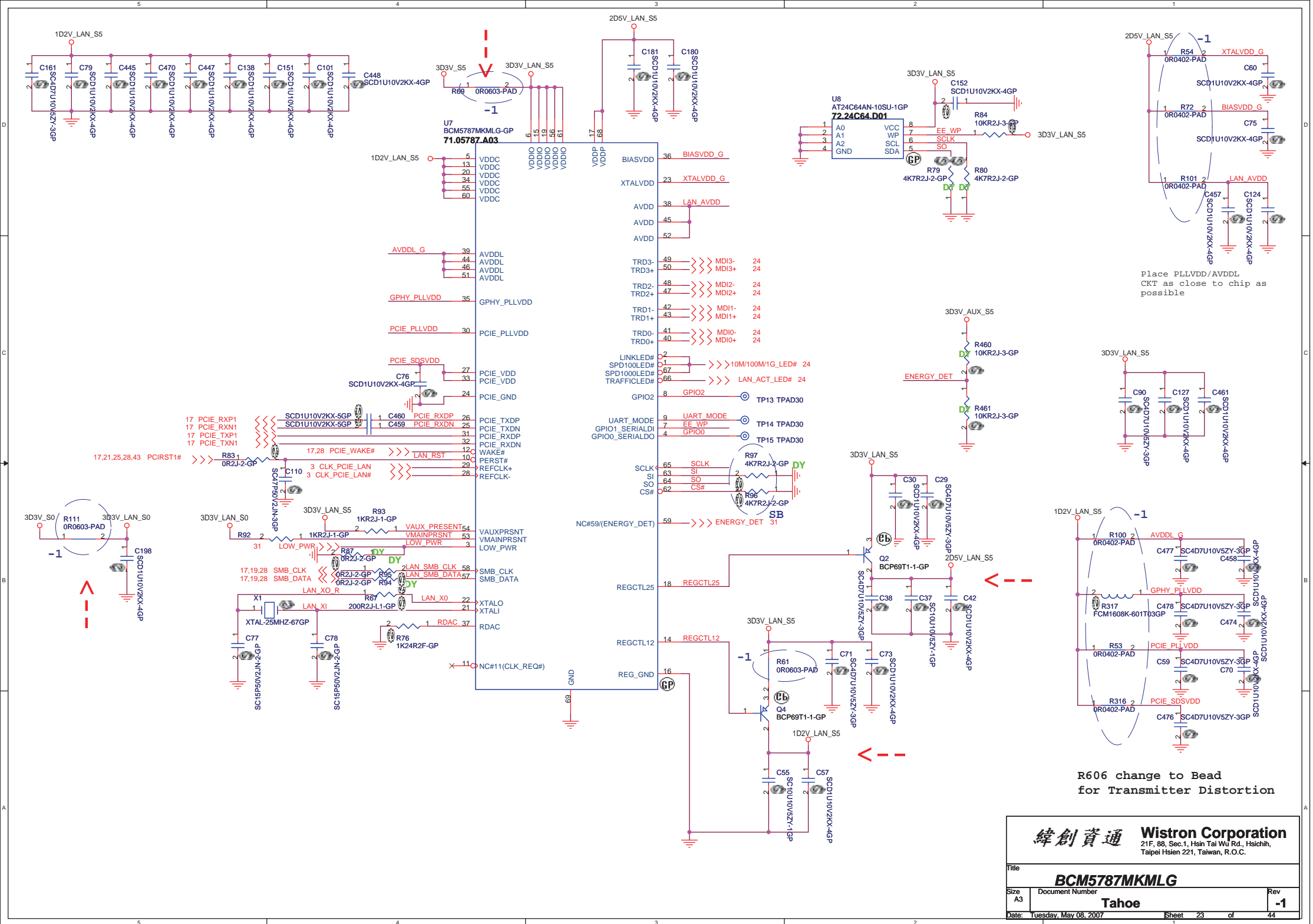
EC21 put near BLUE1 / all USB put one choke near connector by EMI request

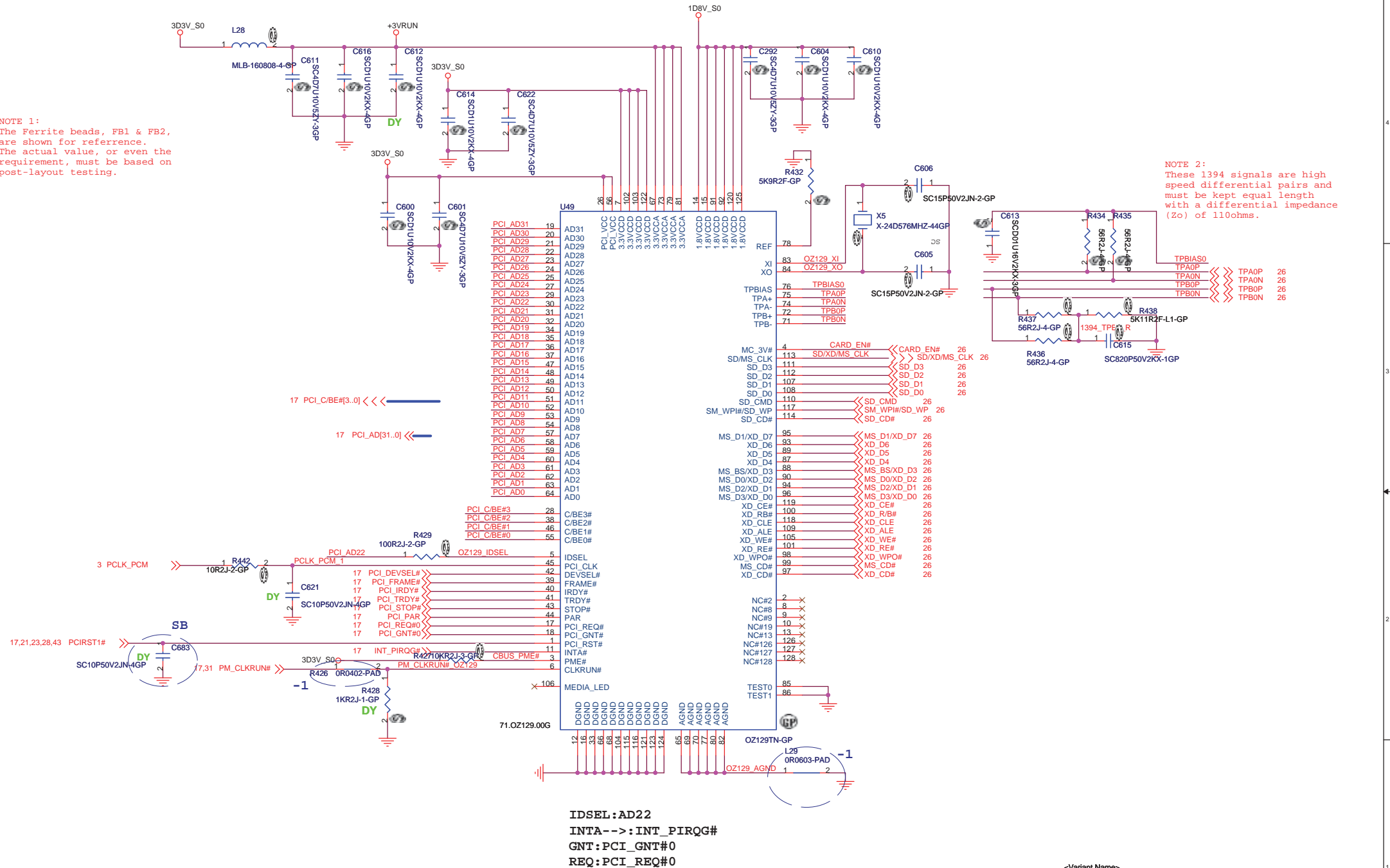
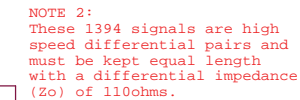
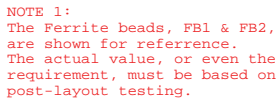
MDC 1.5 CONN



bom1

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Title			
USB / MDC / BLUETOOTH			
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<Variant Name>

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[illegible]

OZ129T

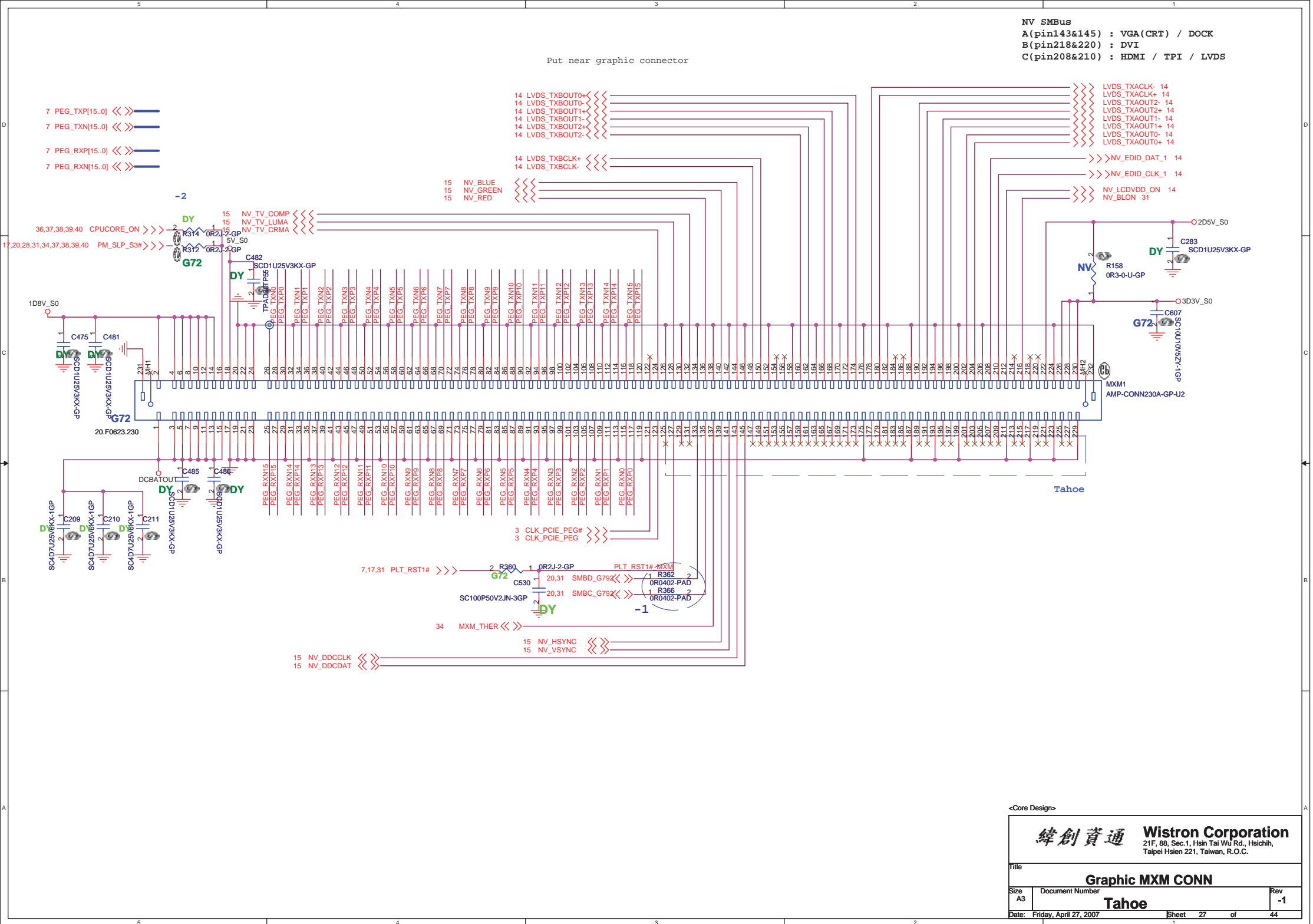
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Tahoe

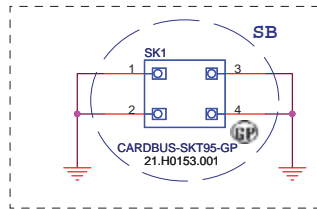
Date: Friday, April 27, 2007

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-1

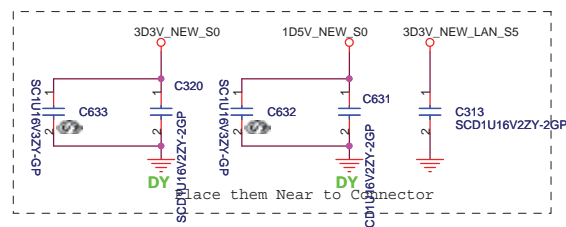
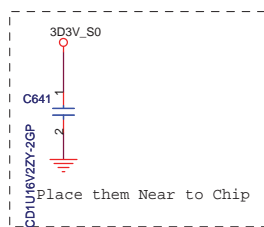
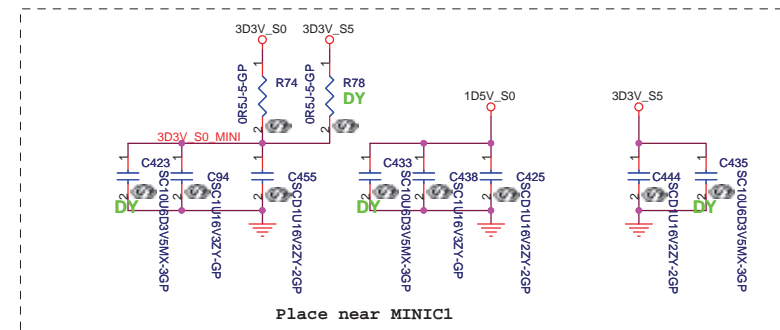
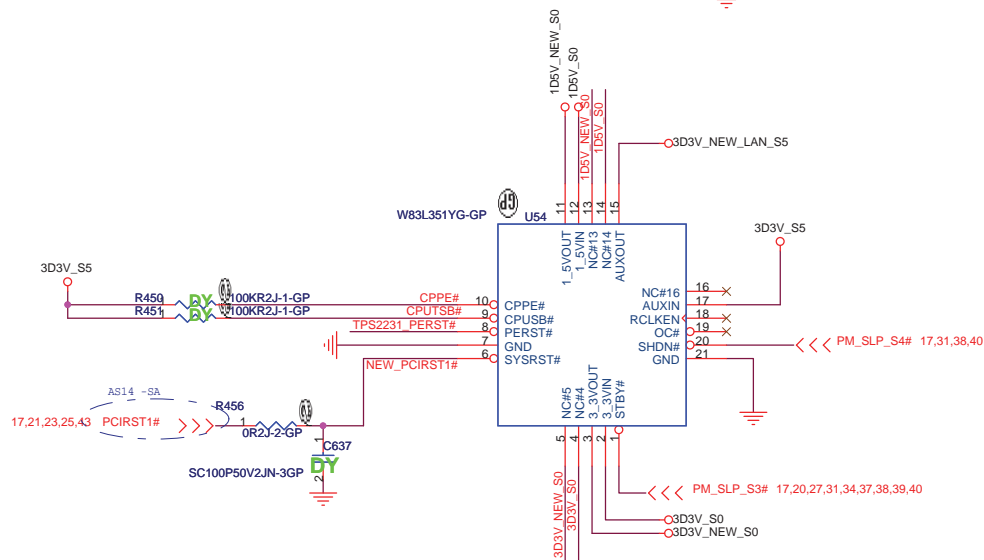
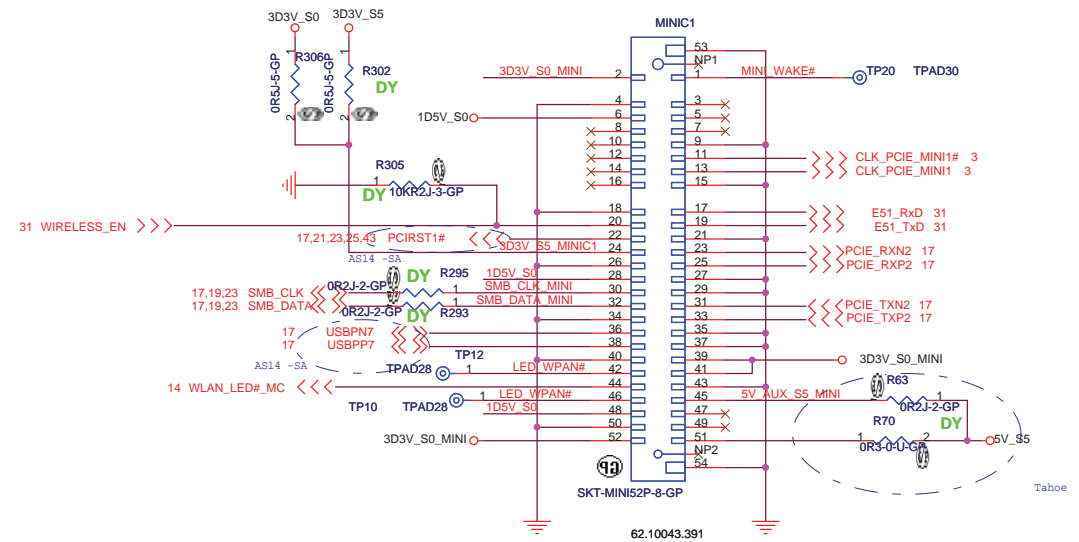


Mini Card Connector



NEWCARD Connector

Reserve the symbol
for bottom side
connector

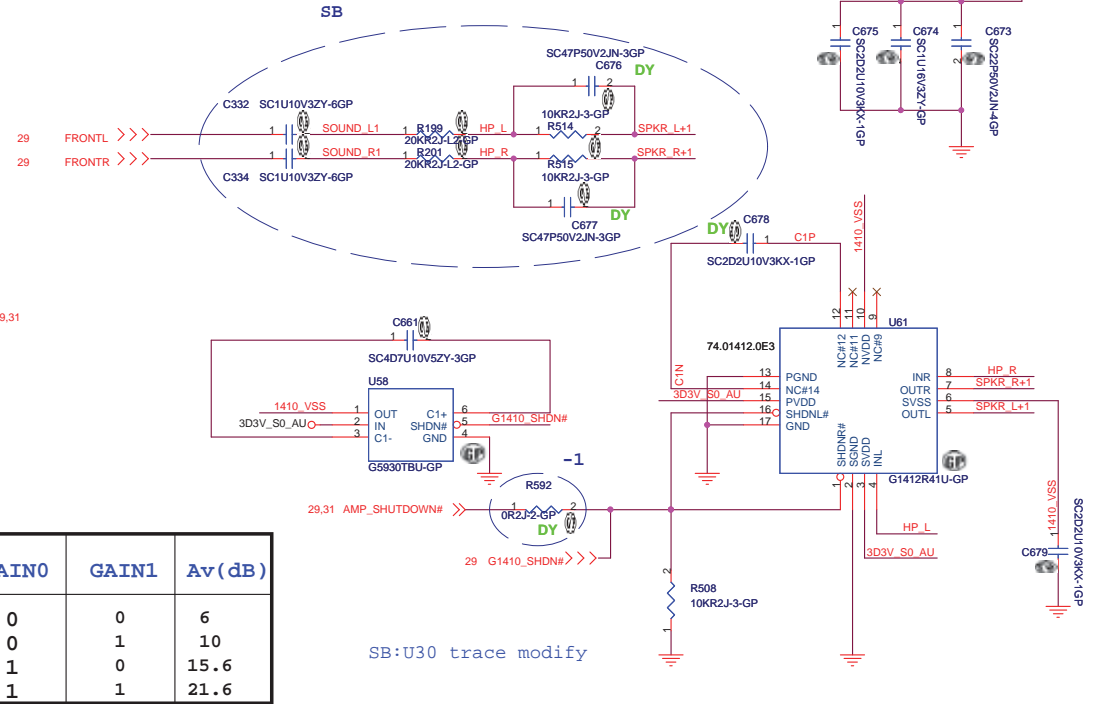


bom1

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Title			
MINI CARD / NEW CARD			
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	Tahoe		-1
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KBC_MUTE_GPIO8



GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

SB:U30 trace modify

R,L 2W Speaker

[illegible]

MIC IN

29 AUD_MICIN_R <<< 2 1 R510 1KR2J-1-GP 1

29 AUD_MICIN_L <<< 2 1 R511 1KR2J-1-GP 1

2 1 R512 1KR2J-1-GP 1

2 1 R509 10KR2J-3-GP 1

2 1 DTDY 10KR2J-3-GP 1

29 MIC_ID# <<< 2

AUD_MIC R

AUD_MIC L

EC119 SC1KP50V2KX-1GP

EC118 SC1KP50V2KX-1GP

MICIN1

PHONE_JK233-GP

22.10133.B01

[illegible]

SPKR L-
SPKR L+
SPKR R-
SPKR R+

SPKR1

1
2
3
4

MLX-COM4-15-GP
20.F0693.004

SB

-1

DY DY

EC131 SC100P50V/2AN-3GP
EC133 SC100P50V/2AN-3GP
EC138 SC100P50V/2AN-3GP
EC13Z SC100P50V/2AN-3GP

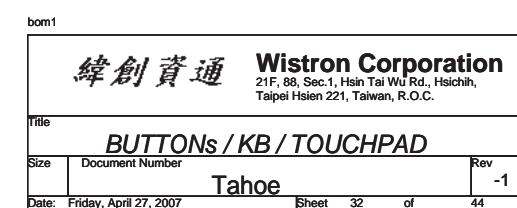
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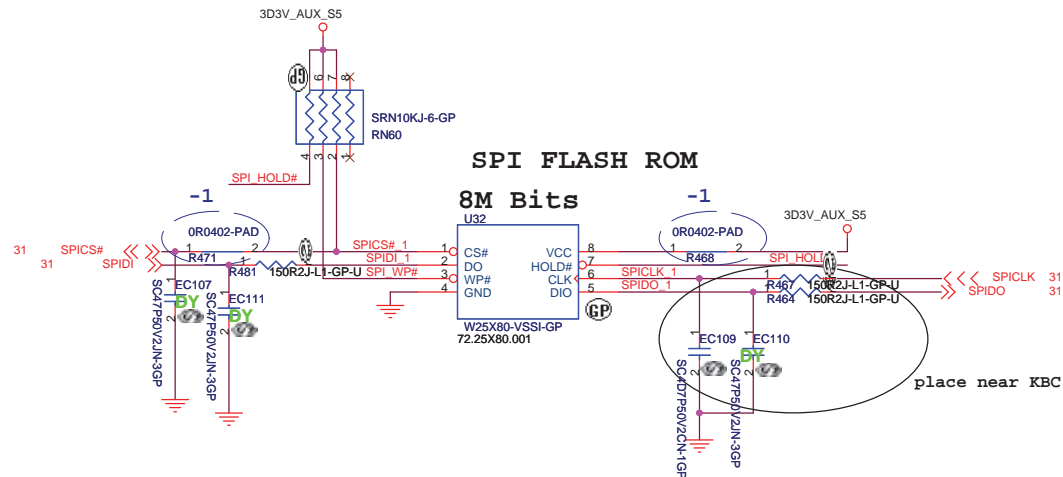
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緯創資通

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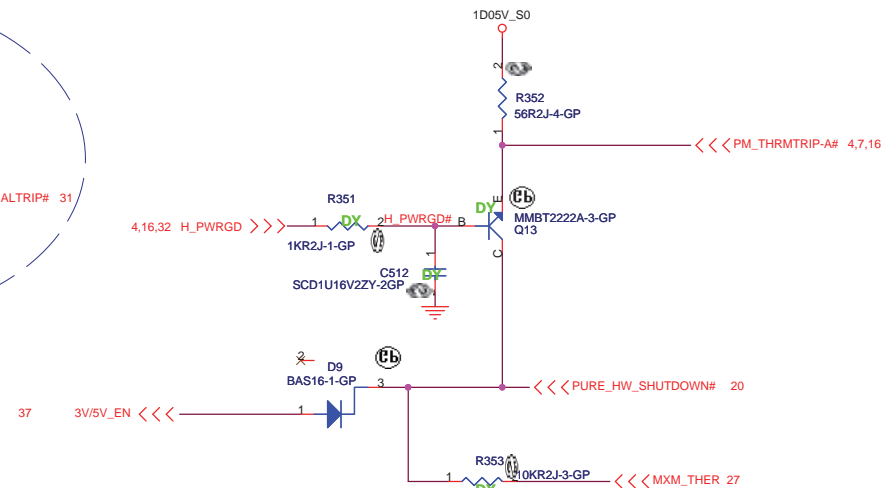
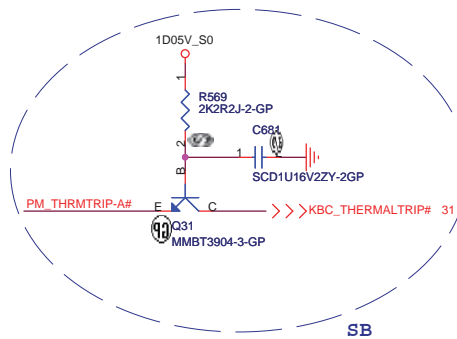
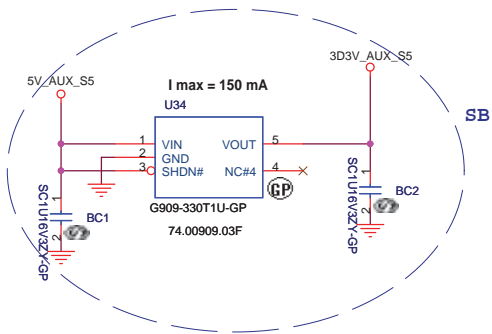




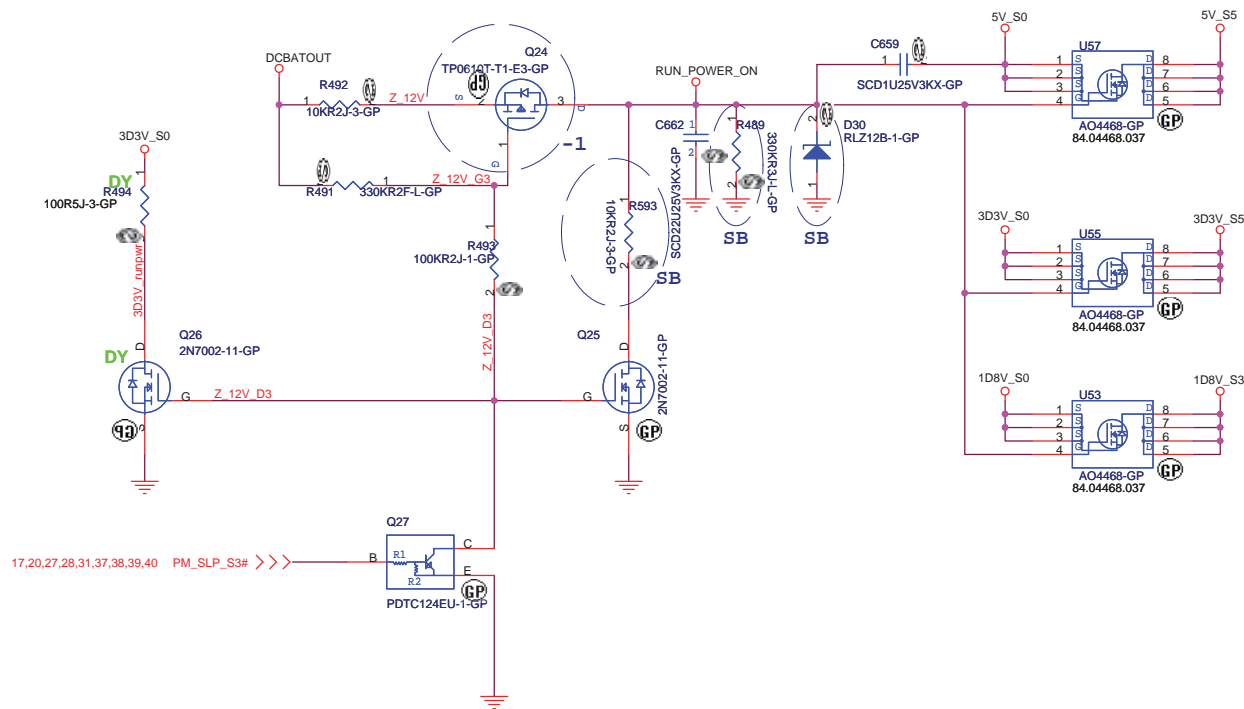
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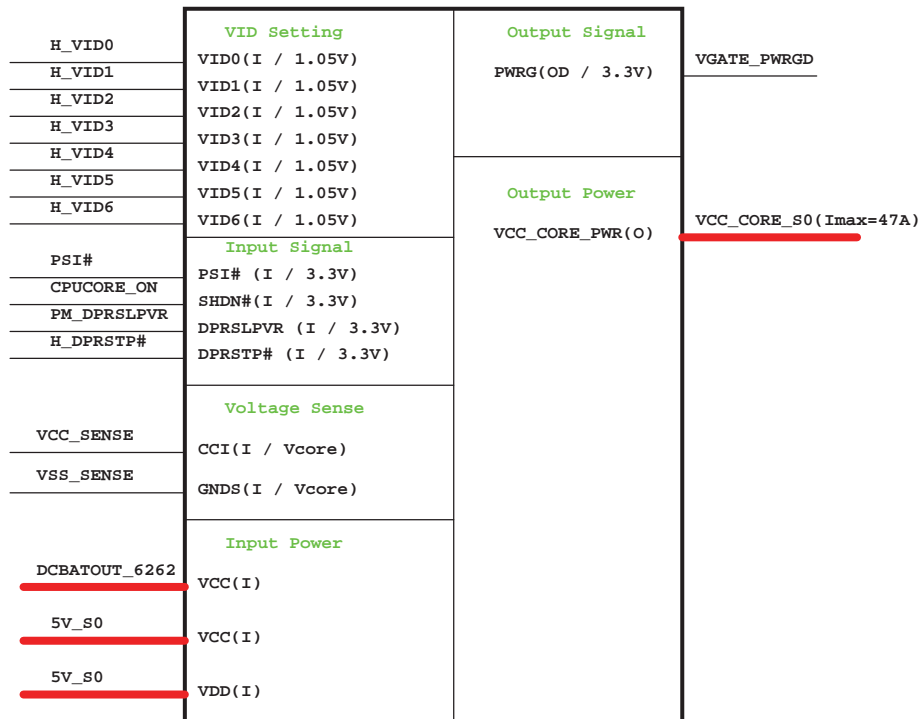
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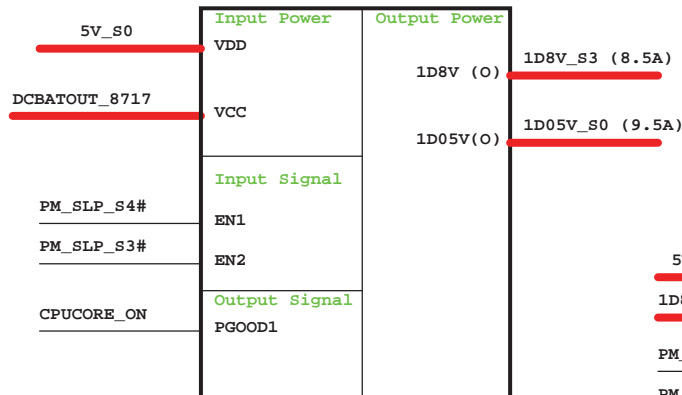
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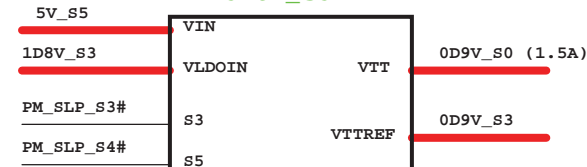
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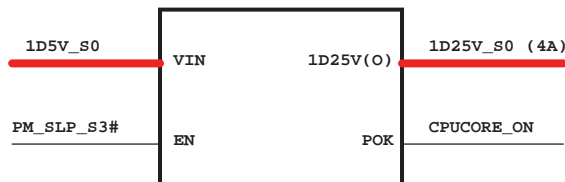


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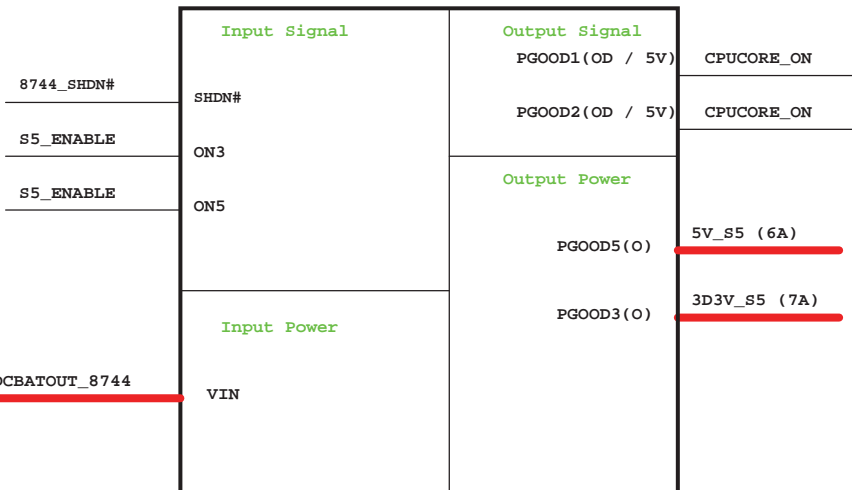
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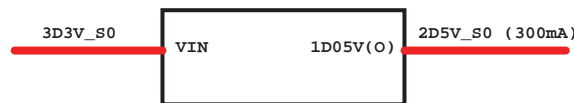


APL5915

MAX8744
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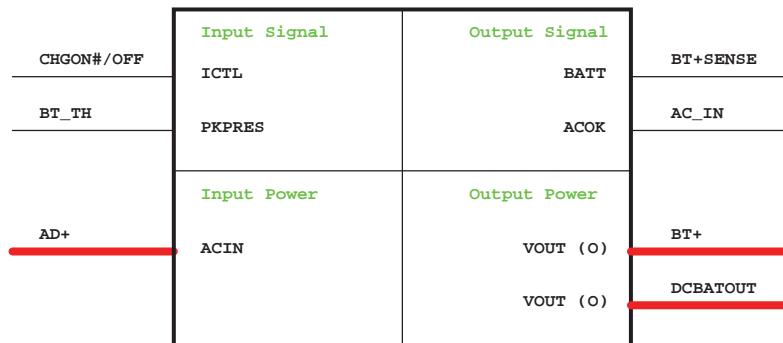


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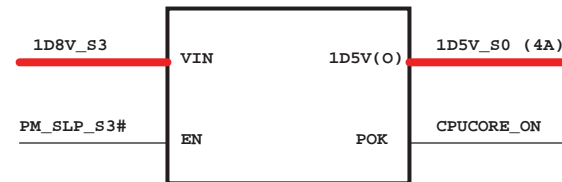


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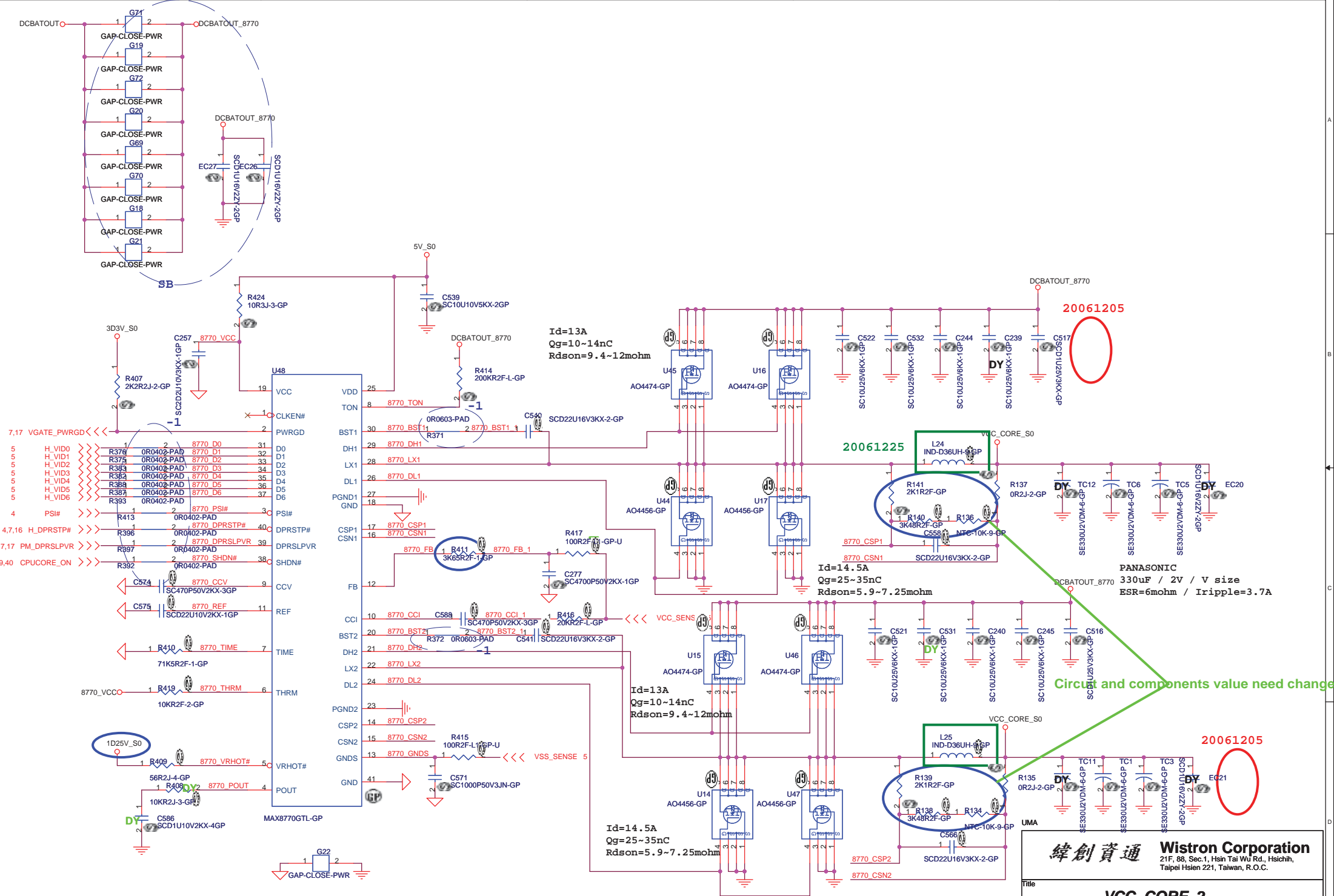


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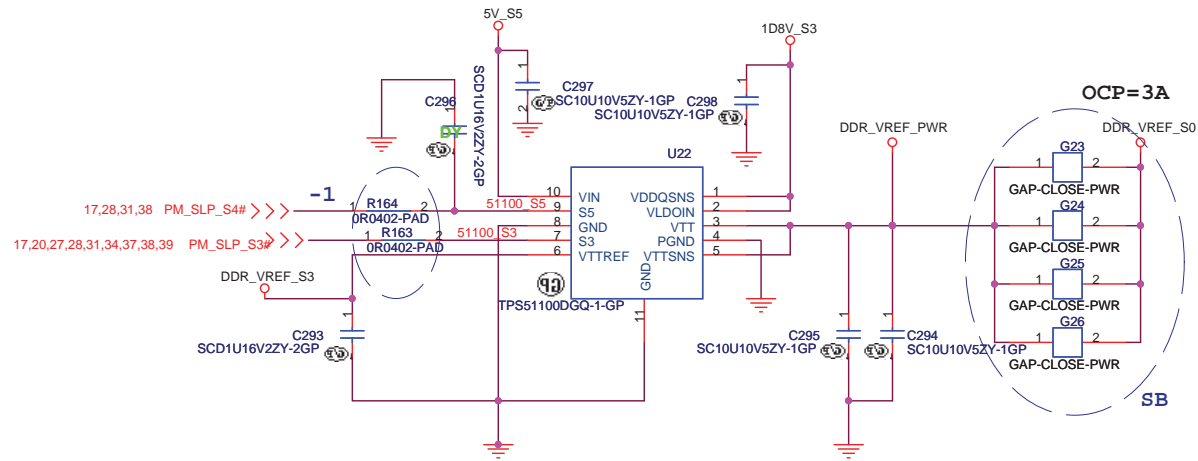
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Power Block Diagram			
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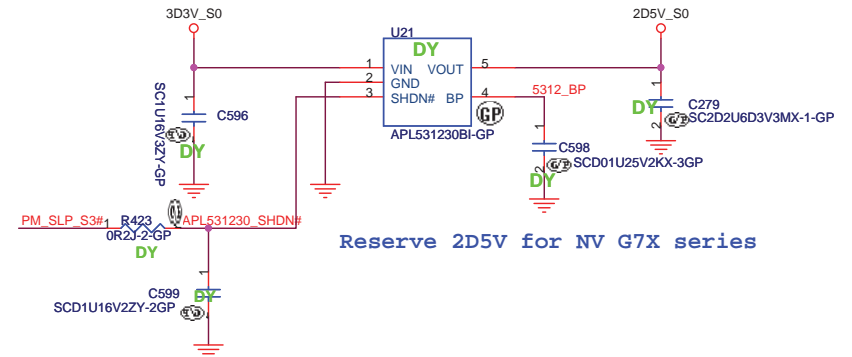
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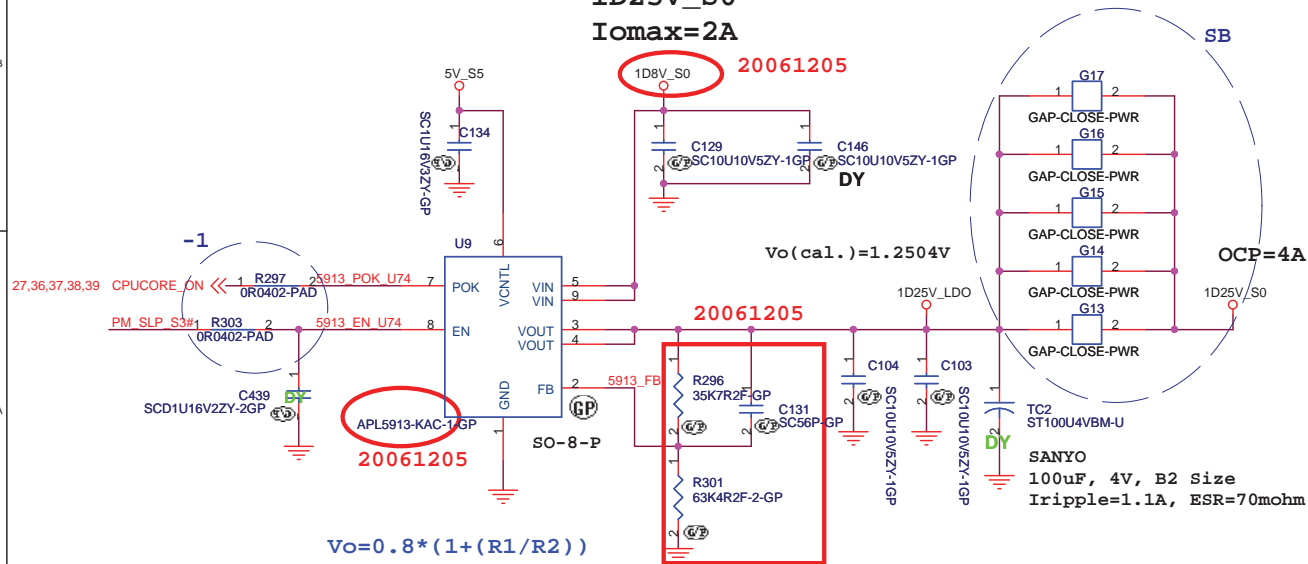
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2D5V
I_{omax}=130mA



1D25V_S0
Iomax=2A



UMA

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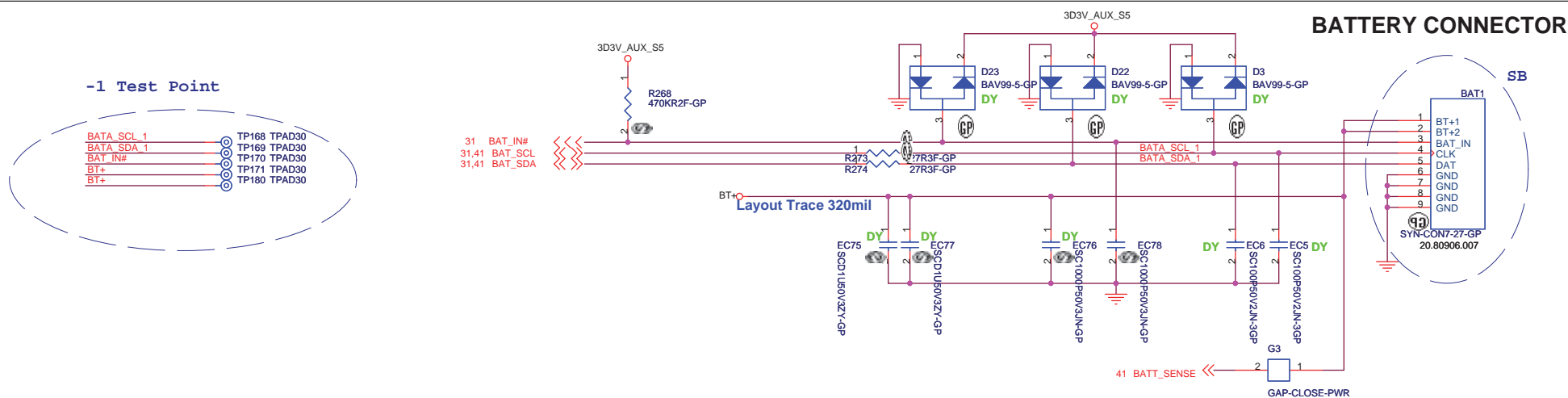
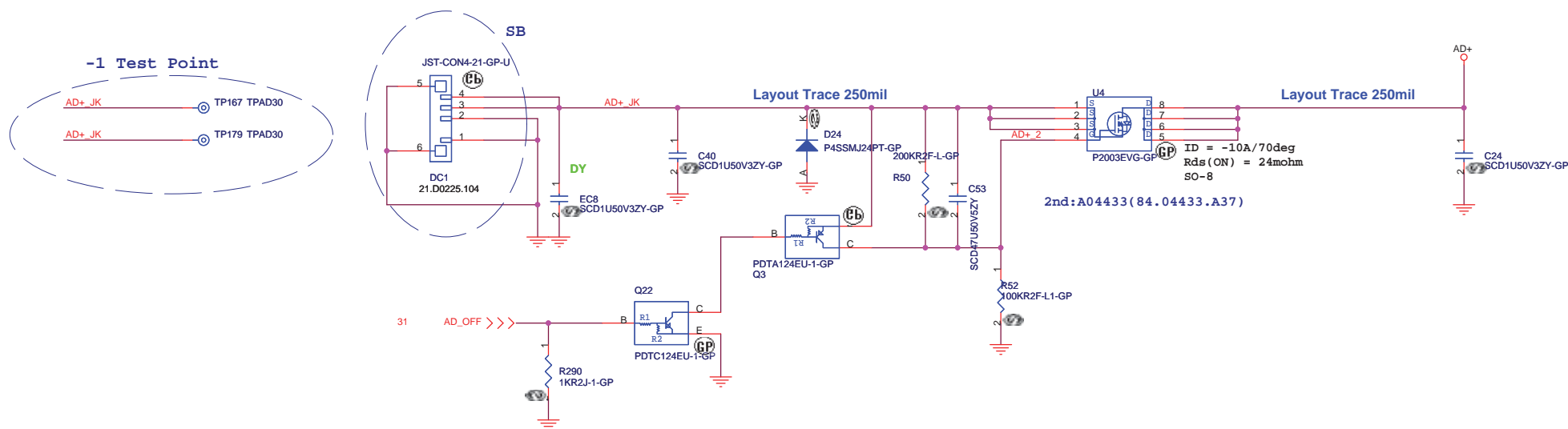
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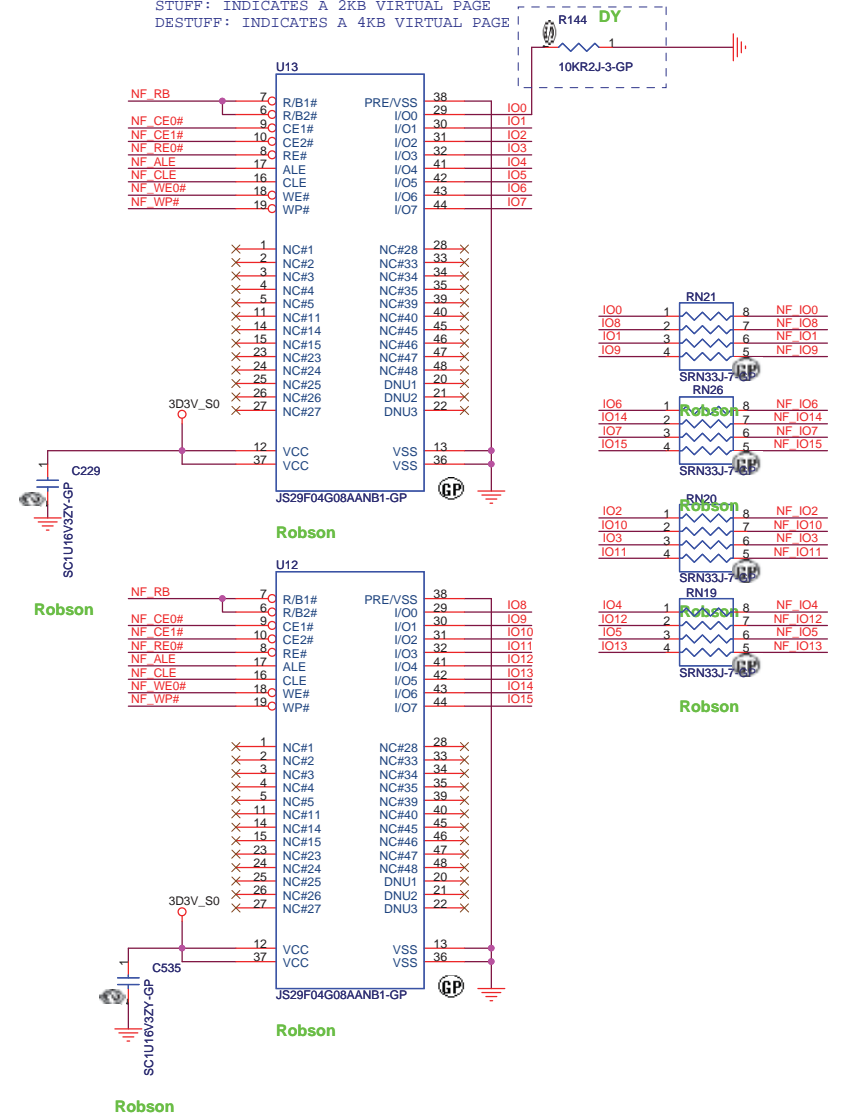
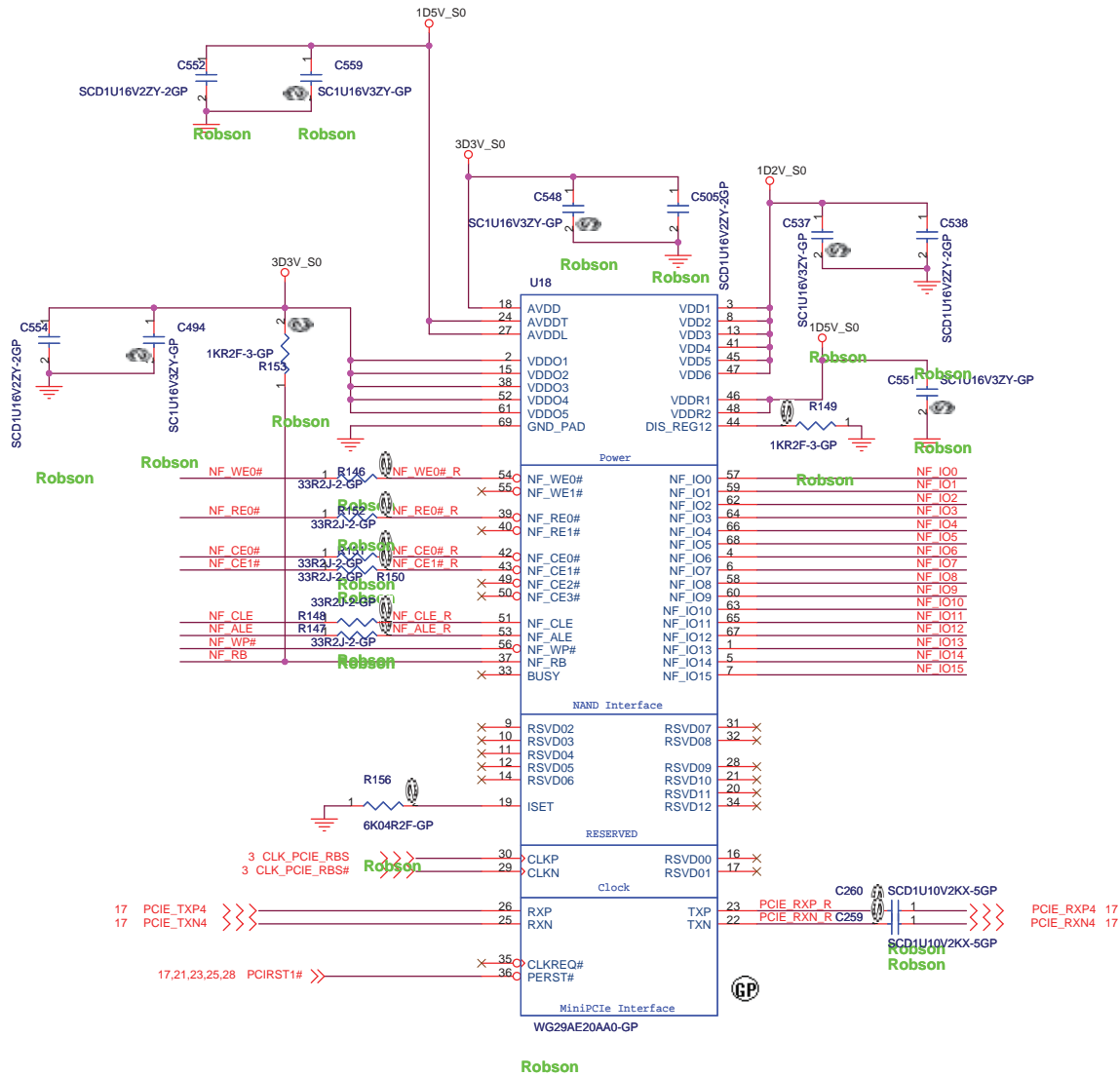
Adaptor in to generate DCBATOUT



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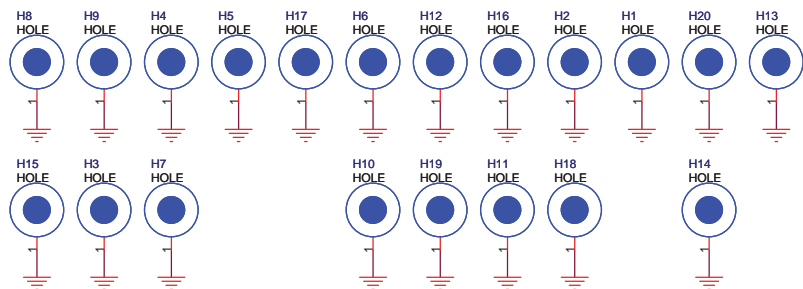
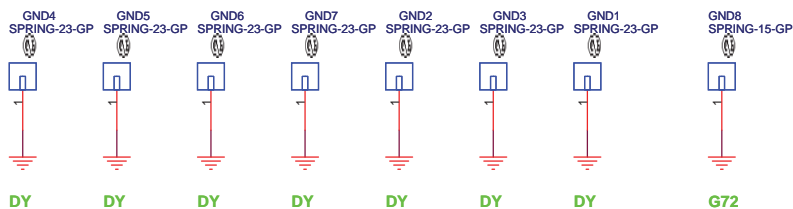
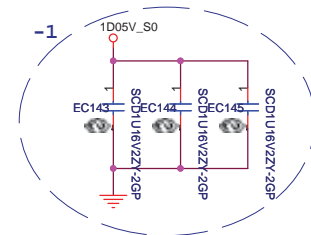
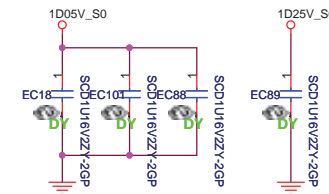
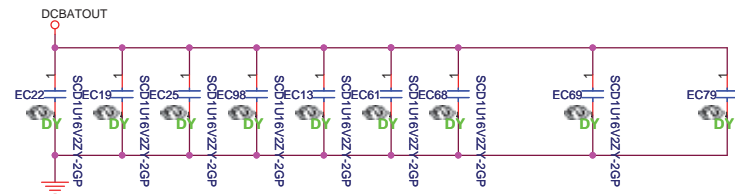
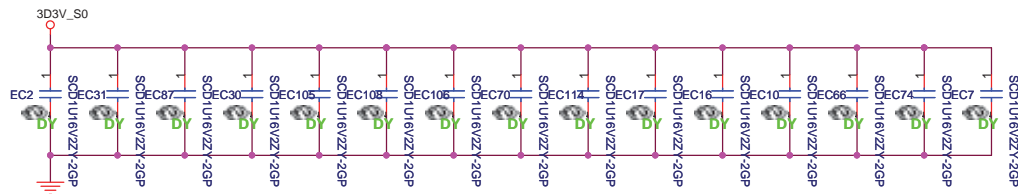
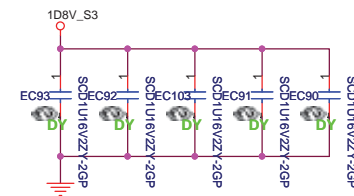
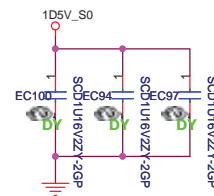
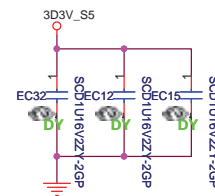
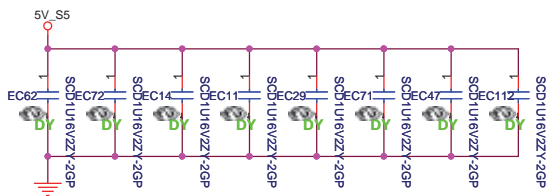
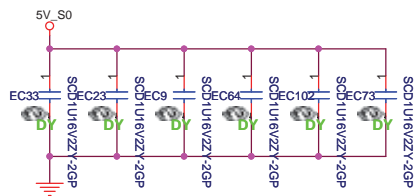
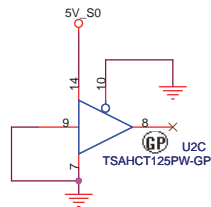
R632
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EMI/Spring/Boss		Tahoe	